Patent Right	Date	March 28, 2022	Court	Intellectual Property High Court, Fourth Division
	Case number	2020 (Gyo-Ke) 10146		
- A case in which the court determined that although there is the omission of a composition in the determination of the primary prior art made by the JPO Decision, the composition does not constitute a difference from the Invention. - A case in which the court determined that although the JPO Decision overlooked a difference, since a person skilled in the art could have easily conceived of the difference based on common general technical knowledge at the time of the priority date, the oversight does not have an impact on the conclusion of the JPO Decision.				

Case type: Rescission of Patent Revocation Decision

Result: Dismissed

References: Article 29, paragraph (2) of the Patent Act

Related rights, etc.: Patent Application No. 2016-567850, Patent No. 6348992, Opposition No. 2018-701050

Summary of the Judgment

1. The case is outlined below.

(1) The Plaintiff filed a patent application (Patent Application No. 2016-567850; hereinafter referred to as the "Application") for an invention titled "TDI line image sensor" for which the international application date was May 14, 2015 (priority date: May 15, 2014 (hereinafter referred to as the "Priority Date"); priority country: Korea), and obtained patent right registration (Patent No. 6348992; number of claims: 1; hereinafter the patent is referred to as the "Patent") on June 8, 2018.

(2) An opposition to a granted patent concerning the Patent (Opposition No. 2018-701050) was filed.

In response to notifications of reasons for revocation, the Plaintiff repeatedly requested corrections. However, the Plaintiff received a notification of reasons for revocation on February 7, 2020, and requested the correction of statements in the claims and the description in question (the "Description") (hereinafter the correction related to this request is referred to as the "Correction") as of May 13, 2020.

Subsequently, the Japan Patent Office approved the Correction on August 18, 2020 and made the decision that "the patent related to Claim 1 of Patent No. 6348992 shall be revoked" (hereinafter referred to as the "JPO Decision").

(3) The Plaintiff filed this lawsuit to seek rescission of the JPO Decision on December

24, 2020.

2. The summary of the JPO Decision is as follows: the Invention could have been easily conceived of by a person skilled in the art based on an invention stated in the description of US Patent No. 7796174, which is a publication distributed before the Priority Date (hereinafter the invention is referred to as "Exhibit Ko 2 Invention"); and therefore, it is an invention for which a patent cannot be granted pursuant to the provisions of Article 29, paragraph (2) of the Patent Act.

3. The Plaintiff alleged that the difference in the Invention was overlooked in the comparison between the Invention and Exhibit Ko 2 Invention; this overlooking has an impact on the conclusion of the decision as to whether a person skilled in the art could have easily conceived of the Invention; and therefore, the JPO Decision contains an error in its determination concerning the lack of an inventive step. Based on this allegation, the Plaintiff sought rescission of the JPO Decision.

4. This judgment explained as follows and determined that all of the reasons for rescission alleged by the Plaintiff are groundless.

(1) Exhibit Ko 2 states, in addition to the composition found by the JPO Decision, that "after charges accumulated in each sense node 804 are sensed multiple times, the signal charge packet of each sense node 804 may be removed" (composition of 2d').

As to whether the signal charge packet that is sensed in the composition of 2d' in Exhibit Ko 2 Invention refers to a single packet or multiple packets, it is not clear based on the statement corresponding to this composition in Exhibit Ko 2. However, according to statements on other embodiments, Exhibit Ko 2 Document is based on the assumption of a composition for sensing a single signal charge packet if being sensed multiple times, and there is no special statement or suggestion about a composition for sensing multiple signal charge packets multiple times. Then, the composition of 2d' means that after charges of a single signal charge packet accumulated in each sense node 804 are sensed multiple times, there are cases where the signal charges of each sense node 804 may be removed."

On the assumption of the composition, and in light of the fact that it was common general technical knowledge at the time of the Priority Date, concerning the signal charge sensing method using an FGA type, that after receiving input of signal charges, signal charges are reset before the next signal charges are transferred, as in the case of Exhibit Ko 2 Invention, it can be said that Exhibit Ko 2 Invention also has a composition in the Invention that "the charge storage nodes receive charges of a line sensor as inputs and the charge storage nodes are reset alternately."

Consequently, the composition of 2d' in Exhibit Ko 2 Invention is not different from

that in the Invention.
(2) Based on FIG. 12 in Exhibit Ko 2 Invention, it must be said that the number of analog-digital converters that are input from the amplifier 1208 is unknown. In this regard, Exhibit Ko 2 Invention is different from the Invention wherein the numbers of amplifiers and AD converters are the same (Difference 3 alleged by the Plaintiff). Consequently, there is Difference 3 between the Invention and Exhibit Ko 2 Invention, in addition to the differences found by the JPO Decision. Therefore, the JPO Decision overlooked Difference 3.

However, it is common general technical knowledge at the time of the Priority Date that AD converters in a solid-state imaging device are arranged in a correspondence relationship of one-to-one to the pixel columns in some cases. Exhibit Ko 2 Invention has a composition wherein the number of multiple sub-arrays 1204, the number of sense nodes, and the number of amplifiers 1208 are the same. Even if the number of AD converters that convert each signal that are output from M pieces of amplifiers is unknown, a person skilled in the art could have easily conceived of the fact based on the aforementioned common general technical knowledge that Exhibit Ko 2 Invention has a composition wherein the number of amplifiers and the number of AD converters are the same.

Then, it cannot be said that the overlooking of Difference 3 above has an impact on the conclusion as to whether the invention could have been easily conceived of by a person skilled in the art.

Judgment rendered on March 28, 2022
2020 (Gyo-Ke) 10146, Case of seeking rescission of patent revocation decision
Date of conclusion of oral argument: February 2, 2022

Judgment

Plaintiff: Vieworks Co., Ltd.

Defendant: Commissioner of the Japan Patent Office

Main text

1. The claim of the Plaintiff shall be dismissed.
2. The Plaintiff shall bear the court costs.
3. The additional time frame for final appeal and for petition for acceptance of final appeal against this judgment shall be thirty days.

Facts and reasons

No. 1 Claim

The decision made by the Japan Patent Office (JPO) on August 18, 2020, concerning Opposition No. 2018-701050 shall be rescinded.

No. 2 Outline of the case

1. Outline of procedures at the JPO (There are no disputes between the parties.)

(1) The Plaintiff filed a patent application (Patent Application No. 2016-567850; hereinafter referred to as the "Application") for an invention titled "TDI line image sensor" for which the international application date was May 14, 2015 (priority date: May 15, 2014 (hereinafter referred to as the "Priority Date"); priority country: Korea) and obtained patent right registration (Patent No. 6348992; number of claims: 1; hereinafter the patent is referred to as the "Patent") on June 8, 2018.

(2) Recrear Inc. filed an opposition to a granted patent on December 25, 2018, concerning the Patent (Opposition No. 2018-701050).

(3) The Plaintiff received a notification of reasons for revocation on March 18, 2019, and, therefore, requested correction of statements in the claims and the description attached to a form in the Application (hereinafter the description is referred to as the "Description") as of June 24, 2019. However, the Plaintiff received another notification

of reasons for revocation on August 29, 2019, and, therefore, requested correction of statements in the claims and the Description as of December 4, 2019 again. However, the Plaintiff received another notification of reasons for revocation again on February 7, 2020, and, therefore, requested correction of statements in the claims and the Description (hereinafter the correction related to this request is referred to as the "Correction") as of May 13, 2020.

Subsequently, the JPO approved the Correction on August 18, 2020, and made the decision that "the patent related to Claim 1 of Patent No. 6348992 shall be revoked" (hereinafter referred to as the "JPO Decision") (additional time frame of ninety days) and its certified copy was sent to the Plaintiff on September 1, 2020.

(4) The Plaintiff filed this lawsuit to seek rescission of the JPO Decision on December 24, 2020.

2. Statement of the claims

(1) Statements in Claim 1 of the claims after the Correction are stated as follows (hereinafter the invention related to Claim 1 after the Correction is referred to as the "Invention").

[Claim 1]

A TDI line image sensor that is characterized by comprising: a pixel unit including N pieces of line sensors having M pieces of CCDs arranged in a line, wherein the N pieces of line sensors are arranged horizontally in the scan direction, configured to horizontally move charges accumulated in the respective columns of the line sensors and accumulate the charges and

an output unit configured to receive the charges accumulated in the pixel unit from the respective columns in parallel as inputs, perform AD conversion on the charges, store the charges, and then sequentially output the charges;

wherein the output unit includes

M pieces of amplifiers configured to receive the charges accumulated in the pixel unit from the respective columns in parallel as inputs at a charge storage node and respectively amplify the charges;

M pieces of AD converters configured to respectively perform AD conversion on signals output from the amplifiers; and a memory buffer configured to store and sequentially output outputs of the AD converters; wherein the amplifiers are source follower amplifiers in which charges are moved from the last line sensor among N pieces of the line sensors of the pixel unit, the charges are turned on according to accumulated electric potentials of the charge storage nodes, and the voltage values thereof are output;

wherein after the charges that are accumulated in M pieces of the CCDs are accumulated in the charge storage nodes for the respective columns and the accumulated charges are amplified through the source follower amplifiers, AD conversion is performed on the charges through the AD converters and then charges are output, and the charge storage nodes are reset to have a voltage connected to a reset drain provided for the respective columns through a reset gate provided for the respective columns;

and wherein the following operations are implemented alternately: the charge storage nodes receive charges of a line sensor as inputs and the charge storage nodes are reset.

(2) Claim 1 that was described separately by the JPO Decision is as follows:

[I/A] A TDI line image sensor that is characterized by comprising: a pixel unit including N pieces of line sensors having M pieces of CCDs arranged in a line, wherein the N pieces of line sensors are arranged horizontally in the scan direction, configured to horizontally move charges accumulated in the respective columns of the line sensors and accumulate the charges and

[B] an output unit configured to receive the charges accumulated in the pixel unit from the respective columns in parallel as inputs, perform AD conversion on the charges, store the charges, and then sequentially output the charges;

wherein the output unit includes

[C] M pieces of amplifiers configured to receive the charges accumulated in the pixel unit from the respective columns in parallel as inputs at a charge storage node and respectively amplify the charges,

[D] M pieces of AD converters configured to respectively perform AD conversion on signals output from the amplifiers, and

[E] a memory buffer configured to store and sequentially output outputs of the AD converters;

[F] wherein the amplifiers are source follower amplifiers in which charges are moved from the last line sensor among N pieces of the line sensors of the pixel unit, the charges are turned on according to accumulated electric potentials of the charge storage nodes, and the voltage values thereof are output;

[G] wherein after the charges that are accumulated in M pieces of the CCDs are accumulated in the charge storage nodes for the respective columns and the accumulated charges are amplified through the source follower amplifiers, AD conversion is performed on the charges through the AD converters and then charges are output, and the charge storage nodes are reset to have a voltage connected to a reset

drain provided for the respective columns through a reset gate provided for the respective columns;

[H] and wherein the following operations are implemented alternately: the charge storage nodes receive charges of a line sensor as inputs and the charge storage nodes are reset.

3. Summary of the JPO Decision

(1) Common features and differences between the invention stated in the description of US Patent No. 7796174 (Exhibit Ko 2; hereinafter the description is referred to as "Exhibit Ko 2 Document" and the invention is referred to as "Exhibit Ko 2 Invention") that is found by the JPO Decision and is a publication distributed before the Priority Date, the Invention, and Exhibit Ko 2 Invention are stated below.

A. Exhibit Ko 2 Invention

(2f/2a) A TDI imager wherein a CCD imaging sensor array 124 includes a plurality of pixels 604 grouped in a plurality of sub-arrays 1204;

(2b) wherein each column of pixels is associated with a sense node 804 and the sense node 804 comprises a contact to the floating diffusion;

(2c) wherein an amplifier 1208 is associated with each sense node 804 and the amplifier consists of a source follower;

(2d) wherein a reset transistor is associated with each sense node 804 in order to reset the sense node 804 and the reset transistor has a gate and a diode drain associated with V reset; and

(2e) wherein signals from pixels are processed by an analog to digital converter 1220 and then processed by a serializer 1224.

B. Common features and differences

(Common features)

[I/A] A TDI line image sensor that is characterized by comprising: a pixel unit including N pieces of line sensors having M pieces of CCDs arranged in a line, wherein the N pieces of line sensors are arranged horizontally in the scan direction, configured to horizontally move charges accumulated in the respective columns of the line sensors and accumulate the charges and

[B] an output unit configured to receive the charges accumulated in the pixel unit from the respective columns in parallel as inputs, perform AD conversion on the charges, store the charges, and then sequentially output the charges;

wherein the output unit includes

[C] M pieces of amplifiers configured to receive the charges accumulated in the pixel unit from the respective columns in parallel as inputs at a charge storage node and

respectively amplify the charges,
[D] M pieces of AD converters configured to respectively perform AD conversion on signals output from the amplifiers, and
[E'] a means to store and sequentially output the outputs of the AD converters;
[F] wherein the amplifiers are source follower amplifiers in which charges are moved from the last line sensor among N pieces of the line sensors of the pixel unit, the charges are turned on according to accumulated electric potentials of the charge storage nodes, and the voltage values thereof are output;
[G] wherein after the charges that are accumulated in M pieces of the CCDs are accumulated in the charge storage nodes for the respective columns and the accumulated charges are amplified through the source follower amplifiers, AD conversion is performed on the charges through the AD converters and then charges are output, and the charge storage nodes are reset to have a voltage connected to a reset drain provided for the respective columns through a reset gate provided for the respective columns;
[H] and wherein the following operations are implemented alternately: the charge storage nodes receive charges of a line sensor as inputs and the charge storage nodes are reset.
(Differences)
"a means to store and sequentially output the outputs of the AD converters" is a "memory buffer" in the Invention; however, it is a "serializer" in Exhibit Ko 2 Invention.
(2) The determination of the JPO Decision related to the differences is stated below.

The "serializer" in Exhibit Ko 2 Invention is an item "to store and sequentially output the outputs of the AD converters" and it is obvious that this action can be implemented using a "memory."

In addition, the "memory" can also be said to be a "memory buffer." Therefore, the composition related to the difference could have been easily conceived of by a person skilled in the art.

Therefore, since the Invention could have been easily conceived of by a person skilled in the art based on Exhibit Ko 2 Invention, a patent cannot be granted pursuant to the provisions of Article 29, paragraph (2) of the Patent Act and the patent related to Claim 1 of the Patent should be revoked.

(omitted)

No. 4 Judgment of this court

1. Statements in the Description

The Description (after the Correction) has statements as stated in Attachment 1. Taking the statements in Attachment 1 together, it is found that the Description discloses the following.

(1) In a TDI line image sensor, line sensors are arranged as a plurality of stages in a scan direction; charges accumulated in CCDs in each line are moved horizontally to CCDs in the next adjacent line, accumulated until the last line, and then output to a signal processing unit by vertically moving the charges accumulated in the last line; and the data with respect to each cell may be sequentially processed in units of lines. However, when the charges accumulated in CCDs are moved vertically in order to be output to the signal processing unit, since the accumulated charges are transmitted by serially moving the accumulated charges one by one in a stopped state, there is a problem in that it takes a lot of time when the accumulated charges are moved vertically. Specifically, in the TDI line image sensor, since the number of CCDs arranged in series in each line is relatively greater, there is a problem that the accumulated charges move vertically and are output, which causes scanning an image through the TDI line image sensor to take a long time ([0010], [0012] through [0014]).

The "present invention" is provided to address the above-described problems, and embodiments of the present invention are directed to provide a TDI line image sensor including a pixel unit, which accumulates charges through CCDs in a TDI (Time Delay Integration) method, and an output unit, which performs AD conversion on charges accumulated in the CCDs in each column, stores the charges in a memory buffer, and then sequentially outputs the charges, and is thereby capable of improving the resolution and transmission rate and reducing power consumption and noise due to the characteristics of a CCD and a CMOS device ([0015]).

(2) The TDI line image sensor in the "present invention" is characterized by comprising a pixel unit including N pieces of line sensors having M pieces of CCDs arranged in a line, wherein the N pieces of line sensors are arranged horizontally in the scan direction, configured to horizontally move charges accumulated in the respective columns of the line sensors and accumulate the charges, and an output unit configured to receive the charges accumulated in the pixel unit from the respective columns in parallel as inputs, perform AD conversion on the charges, store the charges, and then sequentially output the charges. The output unit in the "present invention" is characterized by including M pieces of amplifiers configured to receive the charges accumulated in the pixel unit from the respective columns in parallel as inputs at a charge storage node and respectively amplify the charges, M pieces of AD converters configured to respectively

perform AD conversion on signals output from the amplifiers, and a memory buffer configured to store and sequentially output the outputs of the AD converters. The amplifier in the "present invention" is characterized as a source follower amplifier ([0016] through [0018]).

2. Statements in Cited Document (Exhibit Ko 2 Document)

Exhibit Ko 2 Document, which is a publication distributed before the Priority Date, has statements as shown in Attachment 2 (translation). According to the statements, it is found that the Cited Document discloses the following.

(1) A. Charge-coupled devices (CCDs) have proven to provide exceptional optical performance. Therefore, high performance photon detectors often feature a CCD sensor. Additionally, in the field of aerospace sensors, it is considered that TDI CCDs are uniquely suited to on orbit observations. CCDs, however, are characterized by relatively high-power consumption. For devices in which high power consumption is a concern, CMOS devices are preferable. However, CMOS photon sensors typically produce a noisier signal than CCD devices, and generally have less desirable optical performance. In addition, it is more difficult to perform the function of TDI in a purely CMOS photon sensor (first column, line 19 through line 47).

Accordingly, it would be desirable to create a photon sensor in which the exceptional optical performance of a CCD photon detector was combined with the low power consumption and dense circuitry packaging available using CMOS processes. Combining the CCD and CMOS processes on a single substrate, however, has proven difficult. In addition, devices created on a single substrate using both CCD and CMOS technologies can suffer from poor image quality because of charge transfer inefficiency and high noise due to non-optimized processes. In order to avoid integrating incompatible fabrication process technologies, devices that utilize a structure formed on the first substrate using the first process (e.g., a CCD photon detector) interconnected to the second substrate using the second process (e.g., a CMOS readout) have been developed. Additionally, it should be noted that charge detection generally can be performed only once with respect to a particular collection of charges. Also, providing an un-amplified or un-buffered signal from the CCD can in many cases result in a degraded signal (first column, line 48 through second column, line 7).

B. The present invention is directed at solving these and other problems and disadvantages of the prior art. At least one embodiment of the present invention is based in part on the fact that the power dissipation in a CCD can be dramatically reduced by extracting data from the CCD at or near the column (parallel) outputs thus removing the power-intensive serial shift registers. Thus the combination of a CCD photon

detector with a CMOS readout circuit would provide significant advantages over the present state of the art (second column, line 13 through line 24).

(2) And Exhibit Ko 2 Document has the following statements: [i] "A CCD imaging sensor array 124 includes a plurality of pixels 604 grouped in a plurality of sub-arrays 1204. Each column (row) of pixels 604 may be associated with a sense node 804 a." (ninth column, line 24 through line 27; FIG. 12); [ii] "the sense node 804 typically comprises a contact to the floating diffusion." (sixth column, line 60 and line 61); and [iii] "As illustrated, an amplifier 1208, formed on the first semiconductor substrate 126, may be associated with each sense node 804." (ninth column, line 30 through line 33; FIG. 12), "the amplifier 1208 may comprise a source follower ... to provide a voltage buffered output." (ninth column, line 39 through line 41). According to these statements, it is found that there are statements on an invention including the following particulars for identifying the invention: "A CCD imaging sensor array 124 includes a plurality of pixels 604 grouped in a plurality of sub-arrays 1204;" (2a); "wherein each column of pixels is associated with a sense node 804 and the sense node 804 typically comprises a contact to the floating diffusion;" (2b); and "wherein an amplifier 1208 is associated with each sense node 804 and the amplifier comprises a source follower;" (2c).

In addition, according to the following statements: "... the signal line 906 for carrying the voltage signal from the sense node 804 to the voltage mode amplifier 820 is associated with a reset switch or transistor 908. ... After being sensed (possibly multiple times), the signal charge packet can be removed through a diode drain (not shown in FIG. 9)." (eighth column, line 46 through line 60) and "As illustrated in FIG. 12, ... reset switches 908 can be formed on the first semiconductor substrate for resetting associated sense nodes 804." (tenth column, line 13 through line 20), and based on FIG. 9 and FIG. 12, it is found that Exhibit Ko 2 Document states an invention including the following particulars for identifying the invention: "wherein a reset transistor is associated with each sense node 804 in order to reset the sense node 804 and the reset transistor has a gate and a diode drain associated with V reset" (2d); "after charges accumulated in each sense node 804 are sensed multiple times, the signal charge packet of each sense node 804 may be removed" (2d').

Next, Exhibit Ko 2 Document states that "the signal from a pixel or the integrated signal from many pixels arranged in a TDI arrangement is then processed by an analog to digital converter (ADC) 1220. ... After the data is digitized by an ADC, it can be digitally processed by a serializer 1224, also formed on the second semiconductor substrate 130." (tenth column, line 30 through line 39). Therefore, it is found that Exhibit Ko 2 Document states an invention with the following particulars for

identifying the invention: "wherein signals from pixels are processed by an analog to digital converter 1220 and then processed by a serializer 1224" (2e). In addition, Exhibit Ko 2 Document states that "In other embodiments, charges may be accumulated in successive pixels 604 during successive integration periods. Substantially, all of these accumulated charges are then transferred into the last well 614. This process is also known to persons skilled in the art as TDI (Time Delayed Integration)." (seventh column, line 10 through line 15). Therefore, it is found that Exhibit Ko 2 Document also states an invention related to "TDI imager."

(3) Based on the above, it is found that Exhibit Ko 2 Document states the following invention: "A CCD imaging sensor array 124 includes a plurality of pixels 604 grouped in a plurality of sub-arrays 1204; wherein each column of pixels is associated with a sense node 804 and the sense node 804 comprises a contact to the floating diffusion; wherein an amplifier 1208 is associated with each sense node and the amplifier comprises a source follower; wherein a reset transistor is associated with each sense node 804 in order to reset the sense node 804 and the reset transistor has a gate and a diode drain associated with V reset; wherein after charges accumulated in each sense node 804 are sensed multiple times, the signal charge packet of each sense node 804 may be removed (underlined by this court; hereinafter the underlined part is referred to as "composition of 2d'"); and wherein signals from pixels are processed by an analog to digital converter and then processed by a serializer 1224."

3. Common general technical knowledge

(1) A (A) Exhibit Otsu 5 Document, which is a publication distributed before the Priority Date, states as shown in Attachment 3-1. Taking said statements together, the document discloses that a CCD delay line of buried channel CCD (BCCD), which adopted an FGA type and comprises a charge transfer device that is used in a solid-state imaging device, reads and processes signal charge q1 once during time points t1 through t4, discards the signal charge at t5, transfers new signal charge q2 at t6, and the same processes as for q1 are repeated with signal charge q2.

(B) Exhibit Otsu 6 Document, which is a publication distributed before the Priority Date, states as shown in Attachment 3-2. Taking said statements together, it is found that the document discloses that, in devices related to charge detectors, etc. of CCD, the signal charge Q transferred to a floating gate is absorbed by an RD99 before the next signal charge is transferred, and the next signal charge input is received after the previous signal charge is reset.

(C) Exhibit Otsu 7 Document, which is a publication distributed before the Priority Date, has statements as shown in Attachment 3-3. Taking the statements together, it is

found that the Document discloses that, in a solid-state imaging device that adopted an FGA type as a charge detection method, after reading out a signal charge, the reset gate 26 is set to High and the charge is discharged from the channel region 21 to the reset drain 27.
B. Considering the statements of the documents mentioned in A. (A) through (C) above together, it is found to be common general technical knowledge at the time of the Priority Date that, in a solid-state imaging device using a CCD as imaging elements, if an FGA type is adopted as a signal charge detection method, after receiving an input of a signal charge, the signal charge is reset before the next signal charge is transferred.
C. On the other hand, the Plaintiff alleged as follows, as stated in No. 3, 1 (2) C. (A) above: Exhibit Ko 2 Invention is an FGA type; however, it cannot be said that the invention stated in Exhibit Otsu 7 Document is an FGA type; and therefore, these cannot be evidence to find common general technical knowledge adopted in Exhibit Ko 2 Invention; even if it is an FGA type, there is no disclosure of matters corresponding to the "reset of the floating gate 904" in Exhibit Ko 2 Invention; and Exhibit Otsu 6 Document has no disclosure related to the reset of the floating gate 904 in Exhibit Ko 2 Invention, and therefore, it cannot be evidence to find common general technical knowledge adopted in Exhibit Ko 2 Invention.

However, Exhibit Otsu 7 Document has the following statements: "although the signal charge detection unit is basically a type of an FG method, it is possible to obtain a higher conversion gain than an FG method." ([0011]) and "although the solid-state imaging device 1 is basically a type of a solid-state imaging device using an FG method, it is possible to obtain a higher conversion gain than an FG method." ([0020]). These are based on the assumption that a signal charge detection unit in a solid-state imaging device, which is adopted in the document, adopted an FGA type.

In addition, common general technical knowledge is based on the assumption of various compositions adopted by multiple documents that are technically common, and finds common technical matters that can be extracted. The aforementioned allegation of the Plaintiff only questions the fact that the composition adopted in Exhibit Ko 2 Invention is not disclosed in Exhibit Otsu 6 Document and Exhibit Otsu 7 Document. Therefore, the allegation of the Plaintiff is not adopted.
(2) A. The following publications distributed before the Priority Date have the following statements:
(A) Unexamined Patent Application Publication No. 2007-281540 (Exhibit Ko 24; publication date: October 25, 2007)
"[0001]

The present invention relates to a physical quantity distribution detector and an imaging device, in particular, a physical quantity distribution detector equipped with a column parallel AD (analog-digital) converter and an imaging device in which a solid-state imaging device, which is the physical quantity distribution detector, is used as an imaging device.

[0076]

In the aforementioned embodiments, the invention was described by using a case where the invention is applied to AD converters in which ADC 23 (23-1 through 23-m) including comparator 31 are arranged for the number of pixel columns corresponding to the pixel pitch to signal lines 14-1 through 14-m, in other words, in a correspondence relationship of one-to-one. The present invention is not limited to this application example, but it can be applied in the same way to an AD converter with a composition wherein one ADC 23 is provided for multiple column signal lines 14 and the ADC 23 is used in a time division manner."

(B) Unexamined Patent Application Publication No. 2014-23065 (Exhibit Ko 26; publication date: February 3, 2014)

"[0001]

The present technology is related to a solid-state imaging device and a manufacturing method thereof, in particular, for example, related to a solid-state imaging device and manufacturing method thereof that enables a solid-state imaging device having a plurality of AD converters aligned in the row direction, such as an image sensor equipped with a column-parallel AD conversion unit, etc., to improve crosstalk characteristics between comparators constituting an AD converter between adjacent columns without adverse reactions.

[0308]

In addition, in the present embodiment, in a column-parallel AD conversion unit 22, it was designed to provide one ADC31_n for one line of pixels 11_m and 11_n of a pixel array 10; however, in the column-parallel AD conversion unit 22, for example, one ADC can be provided for a plurality of columns, such as 2 columns of the pixel arrays 11_m and 11_n and AD conversion can be performed with an electric signal from 2 columns of the pixels 11_m and 11_n in one ADC in a time division manner."

(C) Unexamined Patent Application Publication No. 2013-51527 (Exhibit Ko 27; publication date: March 14, 2013)

"[0001]

The present invention relates to a solid-state imaging device and an imaging device.

[0188]

In addition, the first through the fifth embodiments above are described using an example where AD converters including a comparator are arranged for the number of pixel columns corresponding to the pixel pitch, in other words, the AD converters are arranged in a correspondence relationship of one-to-one to the pixel columns. However, the present invention is not limited to this application example. In short, one AD converter may be arranged for a plurality of vertical signal lines 22. In this case, the AD converter performs AD conversion on the signal voltage output to corresponding plurality of vertical signal lines 22 in a time division manner.

B. Considering the statements of the documents mentioned above together, it is found to be common general technical knowledge at the time of the Priority Date that there are AD converters in a solid-state imaging device that are arranged in a correspondence relationship of one-to-one to pixel columns.

4. Overlooking Difference 2 (Grounds for Rescission 1)

(1) The Plaintiff alleged that the JPO Decision overlooked Difference 2 on the assumption that, as stated in No. 3, 1. (2) above, the Invention and Exhibit Ko 2 Invention have differences found by the JPO Decision and that Exhibit Ko 2 Invention has a composition that "After charges accumulated in each sense node 804 are sensed multiple times, the signal charge packet of each sense node 804 may be removed" (2d'). As mentioned in 2. (3) above, Exhibit Ko 2 Invention has the composition of 2d' as alleged by the Plaintiff. Therefore, this point is examined below.

(2) The composition of 2d' of Exhibit Ko 2 Invention corresponds to "After being sensed (possibly multiple times), the signal charge packet can be removed through a diode drain (not shown in FIG. 9)." (eighth column, line 58 through line 60); however, it is not always clear based on this statement whether the sensed signal charge packets refer to a single packet or multiple packets.

Looking at statements related to other embodiments in Exhibit Ko 2 Document, it states concerning the embodiment of FIG. 7 that "... because ... provided with a voltage signal from the sense nodes 804 by the interconnections 404a-b, the voltage of the sense nodes 804 can be read multiple times to provide multiple measurements of a single collection of charge. Accordingly, multiple samples (measurements) can be taken of the charge in or associated with a sense node 804 in order to improve the signal to noise ratio." (seventh column, line 55 through line 63) In short, it states that the voltage of a sense node can be read multiple times whenever one signal charge packet is communicated to a sense node 804. In addition, it states concerning the embodiment of FIG. 8 that "As charges associated with an image signal from one of the pixels 604 are transferred into a potential well 818, voltage changes on a gate 806 are introduced that

can be sensed. ... After being sensed, the signal charge packets can be transferred out of the potential well 818 and removed through a diode 830 and a diode drain 832 or they can remain beneath the floating gate 806 to allow multiple samples for noise reduction. After the desired number of samples is obtained, the charge can then be removed through the diode drain 832." (eighth column, line 23 through line 35). In short, it states that after one signal charge is sensed, the signal charge packets can be removed through the diode drain 832 or they can remain for noise reduction and that after the desired number of samples is obtained, the charges can be removed through a diode drain.

As mentioned above, in Exhibit Ko 2 Document, cases of being sensed multiple times are based on the assumption of a composition for sensing a single signal charge packet, and there is no special statement or suggestion about a composition for sensing multiple signal charge packets multiple times. In this document (sixth column, line 50 through seventh column, line 43), there is a statement of embodiment concerning FIG. 6 that "a summing well 608 may be used just before the sense node 804 in order to improve noise performance." However, there is also no statement concerning "summing" of multiple signal charge packets.

Then, it can be said that the statement in Exhibit Ko 2 Document, "After being sensed (possibly multiple times), the signal charge packet can be removed through a diode drain (not shown in FIG. 9)." (eighth column, line 58 through line 60), is a statement to the effect that after sensing a single signal charge packet multiple times, the signal charge packet may be removed through a diode drain. Therefore, the statement, "after charges accumulated in each sense node 804 are sensed multiple times, the signal charge packet of each sense node 804 may be removed" (composition of 2d') means a composition wherein after charges of a single signal charge packet accumulated in each sense node 804 are sensed multiple times, there are cases where the signal charges of each sense node 804 may be removed.

On the assumption of such composition, and in light of the fact that it was common general technical knowledge at the time of the Priority Date, concerning the signal charge sensing method using an FGA type, that after receiving input of signal charges, signal charges are reset before the next signal charges are transferred, as in the case of Exhibit Ko 2 Invention, it can be said that Exhibit Ko 2 Invention also has a composition in the Invention that "the charge storage nodes receive charges of a line sensor as inputs and the charge storage nodes are reset alternately" (Constituent Feature H).

Consequently, the composition of 2d' in Exhibit Ko 2 Invention is not different from that in the Invention.

(3) On the other hand, the Plaintiff alleged as follows, as stated in No. 3, 1. (2), A. (B) above, based on the assumption that an action to reset after receiving charge input from a line sensor multiple times means to accumulate charge input from multiple lines: as stated in No. 3, 1. (2), C. (B), improvement of noise performance by summing charges of multiple pixels in Exhibit Ko 2 Invention is achieved through the adoption of well-known art, which is called pixel binning; this well-known art conflicts with the common general technical knowledge in question (hereinafter referred to as the "Common General Technical Knowledge"); and therefore, the Common General Technical Knowledge is not used in Exhibit Ko 2 Invention.

However, as stated in (2) above, it can be said that the statement in Exhibit Ko 2 Invention, "After being sensed (possibly multiple times), the signal charge packet can be removed through a diode drain (not shown in FIG. 9)." is a statement to the effect that after sensing a single signal charge packet multiple times, the signal charge packet can be removed through a diode drain. Therefore, the Plaintiff's aforementioned allegation is groundless due to the lack of assumption.

(4) Based on the above, the JPO Decision contains an error in terms of not finding the composition of 2d' in Exhibit Ko 2 Invention; however, since Difference 2 (or Difference 2') alleged by the Plaintiff does not exist, the conclusion of the JPO Decision is reasonable and Grounds for Rescission 1 alleged by the Plaintiff are groundless.

5. Grounds for Rescission 2 (overlooking Difference 3)

(1) As stated in No. 3, 1. (3) above, the Plaintiff alleged that the JPO Decision overlooked Difference 3 in the comparison between the Invention and Exhibit Ko 2 Invention concerning the following point: in the line sensor of the Invention, M pieces of CCDs are arranged in a line and M pieces of amplifiers and M pieces of AD converters are provided, charges accumulated in M pieces of CCDs are received in parallel as inputs and are amplified by M pieces of amplifiers, and each signal output from M pieces of amplifiers is AD-converted by M pieces of the AD converters; on the other hand, in the line sensor in Exhibit Ko 2 Invention, M pieces of the CCDs are arranged in a line and M pieces of amplifiers are provided, but an analog-digital converter is one unit, although charges accumulated in M pieces of CCDs are received in parallel as inputs and are amplified by M pieces of amplifiers, it is not clear whether each signal output from M pieces of the amplifiers is AD-converted by an AD converter. Therefore, this point is examined below.

(2) A. The Invention has the following particulars for identifying the invention: a "line sensor having M pieces of CCDs arranged in a line" (Constituent Feature A); "M pieces of amplifiers configured to receive the charges accumulated in the pixel unit from the

respective columns in parallel as inputs at a charge storage node" (Constituent Feature C); and "M pieces of AD converters configured to respectively perform AD conversion on signals output from the amplifiers, and" (Constituent Feature D). Therefore, it can be said that "the line sensor" in the Invention "has a composition wherein M pieces of CCDs are arranged in a line and M pieces of amplifiers and M pieces of AD converters are provided; charges accumulated in M pieces of CCDs are received in parallel as inputs and are amplified by M pieces of amplifiers; and each signal output from M pieces of the amplifiers is AD-converted by M pieces of AD converters."

On the other hand, Exhibit Ko 2 Invention has the following composition: "A CCD imaging sensor array 124, which is a TDI imager (2f) and includes a plurality of pixels 604 grouped in a plurality of sub-arrays 1204" (2a); "wherein each column of pixels is associated with a sense node 804" (2b); "wherein an amplifier 1208 is associated with each sense node 804" (2c). It can be understood that the composition has the same number of multiple sub-arrays 1204, number of sense nodes, and number of amplifiers 1208. However, based on the composition that "wherein signals from pixels are processed by an analog to digital converter 1220 and then processed by a serializer 1224" (2e), the number of analog-digital converters is not identified. Looking at statements in Exhibit Ko 2 Document, in FIG. 12, a statement of the analog-digital converter 1220 is omitted; it is unknown whether the number of analog-digital converters 1220 is the same as the numbers of sub-arrays 1204, sense nodes, and amplifiers; and there is no statement on how the amplifier 1208 is input to the analog-digital converter 1220.

Then, in Exhibit Ko 2 Invention, it must be said that the number of analog-digital converters that are input from the amplifier 1208 is unknown. In this regard, Exhibit Ko 2 Invention is different from the Invention wherein the numbers of amplifiers and AD converters are the same (Difference 3 alleged by the Plaintiff).

B. On the other hand, the Defendant alleged as follows: as stated in No. 3, 2. (3), A. above, "Amplifier 1216" and three codes of "⋯" that aligned vertically in FIG. 12 of Exhibit Ko 2 Document could have been understood by a person skilled in the art that they mean that there should have been many amplifiers 1216, but they are omitted on the figure; in a TDI imager in Exhibit Ko 2 Invention, reading (sensing) is implemented for each column and, therefore, the charge value that a "sense node 804" in each column accepted is amplified by an "Amplifier 1208" corresponding to each column, is input to the analog-digital converter 1220 and processed at the same time through an amplifier 1216 corresponding one-to-one to the amplifier 1208; and therefore, Difference 3 does not exist.

However, there are the following statements in Unexamined Patent Application Publication No. 1994-197285 (Exhibit Ko 25; publication date: July 15, 1994), in addition to the statements of the documents mentioned in 3. (2) A. above, that "In the second invention, a switching means to switch two color signals obtained from an imaging sensor in a time division manner is provided." ([0018]) and "According to the second invention, an AD converter that is used for recording can be reduced by adding two color signals obtained from the switching means in a time division manner to a common AD converter." ([0020]). Taking together the aforementioned statements, since providing a smaller number of AD converters in a solid-state imaging device than the number of amplifiers was also common general technical knowledge at the time of the Priority Date, the value of charges accepted by a "sense node 804" in each column is not always amplified by the "Amplifier 1208" corresponding to each column, input to the analog-digital converter 1220 and processed at the same time through an amplifier 1216 corresponding one-to-one to the amplifier 1208 and it cannot be said that a person skilled in the art could have naturally understood that the number of analog-digital converters and amplifiers are the same according to the omitted statement of "…" in FIG. 12. Therefore, the Defendant's allegation above is groundless.

(3) As stated in (2) above, there is Difference 3 between the Invention and Exhibit Ko 2 Invention, in addition to the differences found by the JPO Decision. Therefore, the JPO Decision overlooked Difference 3.

However, as stated in 3. (2) above, it is common general technical knowledge at the time of the Priority Date that AD converters in a solid-state imaging device are arranged in a correspondence relationship of one-to-one to the pixel columns in some cases. Exhibit Ko 2 Invention has a composition wherein the numbers of multiple sub-arrays 1204, sense nodes, and amplifiers 1208 are the same. Even if the number of AD converters that convert each signal that is output from M pieces of amplifiers is unknown, a person skilled in the art could have easily conceived of the fact based on the aforementioned common general technical knowledge that Exhibit Ko 2 Invention has a composition wherein the numbers of amplifiers and AD converters are the same.

Then, it cannot be said that the overlooking Difference 3 above has an impact on the conclusion as to whether the invention could have been easily conceived of by a person skilled in the art.

(4) Based on the above, although the JPO Decision overlooked Difference 3, it does not have impact on the conclusion of the JPO Decision and, therefore, Grounds for Rescission 2 alleged by the Plaintiff are groundless.

6. Conclusion

Based on the above, all the grounds for rescission alleged by the Plaintiff are groundless and no illegality that requires the rescission of the JPO Decision can be found. Consequently, the claim of the Plaintiff shall be dismissed, and the judgment is rendered as indicated in the main text.

Intellectual Property High Court, Fourth Division
Presiding judge: KANNO Masayuki
Judge: NAKAMURA Kyo
Judge: OKAYAMA Tadahiro

(Attachment 1)

Description

[Technical Field]

[0001]

The present invention relates to a time delay integration (TDI) line image sensor, and more particularly, to a TDI line image sensor including a pixel unit, which accumulates charges through charge-coupled devices (CCDs) in a TDI method, and an output unit, which performs analog-to-digital (AD) conversion on the charges accumulated in the CCDs in each column, stores the charges in a memory buffer, and then sequentially outputs the charges, and thereby capable of improving resolution and a transmission rate and reducing power consumption and noise due to characteristics of a CCD and a complementary metal-oxide-semiconductor (CMOS) device.

[Background Art]

[0002]

Recently, with mass production, automation, and refinement of production facilities, functions which rely on the naked eye of a person or various types of sensors have been increasingly replaced by vision machines including image sensors. Charge-coupled devices (CCDs) are semiconductor devices that are mainly used in these image sensors.

[0003]

A CCD refers to a device capable of transmitting a charge from one device to another adjacent device. An image sensor including such CCDs has a structure in which a change of an amount of free charges in each cell due to an amount of light is converted into an electrical signal.

[0004]

Structurally, the CCD mainly includes a cell area in which charges are substantially accumulated due to an amount of light, and an output unit including a shift register which serves as a path through which the accumulated charges are sequentially transmitted.

[0005]

The CCDs are divided into an area scan method, a line scan method, a time delay integration (TDI) line scan method, and the like according to a method in which cells are arranged in an array and an image is generated.

[0006]

An image sensor using a line scan method (hereinafter referred to as a "line sensor") is a one-dimensional sensor in which pixels which receive image light are arranged in a line. When a two-dimensionally widened image is imaged, a subject is sequentially

imaged line by line by moving the line sensor or the subject.

[0007]

That is, the line scan method is a method in which one line is exposed and transmitted at an arbitrary speed at a time, and has an advantage in that a high-speed and high-resolution image may be obtained with low cost compared to an area scan method. For example, while 4M pixels are required in the area scan method in order to obtain a frame having a size of 2048 * 2048, frames having various sizes such as 2048 * 2048, 2048 * 1000, and the like may be obtained using only 2K pixels in the line scan method.

[0008]

However, when a high-speed scan method such as a case in which a subject which is moving at a high speed is imaged or a case in which a subject is imaged by moving a line sensor at a high speed is performed, since accumulation and transmission of charges at the high speed are repeated in each line, a time during which the charges may be accumulated per line is reduced, and thus an amount of light of the image becomes insufficient. Thus, demand for an amount of light is increasing, but the amount of light may not be indefinitely increased due to a limitation of a lighting device.

[0009]

Accordingly, while research on increasing sensitivity by improving materials of a pinned-photodiode (PPD), a complementary metal-oxide-semiconductor (CMOS) sensor, and the like has been progressing, a method in which an amount of light is accumulated by arranging several line sensors to increase sensitivity has been proposed.

[0010]

In an image sensor using a TDI line scan method (hereinafter referred to as a "TDI line image sensor"), line sensors are arranged as a plurality of stages in a scan direction, charges accumulated in CCDs in each line are synchronized with movement of an image, and are transmitted to CCDs in a next line. The charges overlap and are then output by repeating the process until the last line sensor, and as a result, an image having a sufficiently satisfactory amount of light may be obtained even in a high-speed scan method.

[0011]

The related art of the present invention is disclosed in Korean Unexamined Patent Application Publication No. 2009-0023573 (published on March 5, 2009; Invention Title: Method for Controlling a TDI-CCD Image Sensor).

[Outline of the invention]

[Problem to be solved by the invention]

[0012]

The present invention is directed to providing a time delay integration (TDI) line image sensor in which charges accumulated in charge-coupled devices (CCDs) in each line are horizontally moved to CCDs in an adjacent next line, are moved to a last line and accumulated, and are then output to a signal processing unit by vertically moving the charges accumulated in the last line, and data with respect to each cell may be sequentially processed in units of lines.

[0013]

As described above, when the charges accumulated in the CCDs are horizontally moved to an adjacent line, the charges are moved in parallel by being synchronized with movement of an image, however, when the accumulated charges are vertically moved in order to be output to the signal processing unit, since the accumulated charges are transmitted by serially moving the accumulated charges one by one in a stopped state, there is a problem in that it takes a lot of time when the accumulated charges are vertically moved.

[0014]

Specifically, in the TDI line image sensor, since the number of CCDs vertically arranged in series in each line is relatively greater than the number of lines horizontally arranged in a scan direction in order to have high resolution, there is a problem in that the accumulated charges vertically moving and being output cause scanning an image through the TDI line image sensor to take a lot of time.

[0015]

The present invention is provided to address the above-described problems, and embodiments of the present invention are directed to providing a TDI line image sensor including a pixel unit, which accumulates charges through CCDs in a TDI method, and an output unit, which performs analog-to-digital (AD) conversion on charges accumulated in the CCDs in each column, stores the charges in a memory buffer, and then sequentially outputs the charges, and thereby capable of improving resolution and a transmission rate and reducing power consumption and noise due to characteristics of a CCD and a complementary metal-oxide-semiconductor (CMOS) device.

[Means for solving the problem]

[0016]

One aspect of the present invention provides a time delay integration (TDI) line image sensor, the sensor including a pixel unit including N pieces of line sensors having M pieces of charge-coupled devices (CCDs) arranged in a line, wherein the N pieces of line sensors are arranged horizontally in a scan direction, configured to horizontally

move charges accumulated in respective columns of the line sensors and accumulate the charges, and an output unit configured to receive the charges accumulated in the pixel unit from the respective columns in parallel as inputs, perform analog-to-digital (AD) conversion on the charges, store the charges, and then sequentially output the charges.

[0017]

The output unit may include M pieces of amplifiers configured to receive the charges accumulated in the pixel unit from the respective columns in parallel as inputs at a charge storage node and respectively amplify the charges, M pieces of AD converters configured to respectively perform AD conversion on signals output from the amplifiers, and a memory buffer configured to store and sequentially output outputs of the AD converters.

[0018]

The amplifiers of the present invention may be source follower amplifiers.

[Advantageous Effects]

[0019]

A time delay integration (TDI) line image sensor according to the present invention includes a pixel unit, which accumulates charges through charge-coupled devices (CCDs) in a TDI method, and an output unit which performs analog-to-digital (AD) conversion on charges accumulated in CCDs in each column, stores the charges in a memory buffer, and then sequentially outputs the charges, and thus resolution and a transmission rate can be improved and power consumption and noise can be reduced due to characteristics of a CCD and a complementary metal-oxide-semiconductor (CMOS) device.

[Description of Drawings]

[Mode for Working the Invention]

[0023]

FIG. 1 is a block diagram illustrating the TDI line image sensor according to one embodiment of the present invention, FIG. 2 is a view illustrating a structure of a pixel unit of the TDI line image sensor according to one embodiment of the present invention, and FIG. 3 is a view for describing movement of charges in the TDI line image sensor according to one embodiment of the present invention.

[0024]

As illustrated in FIGS. 1 and 2, the TDI line image sensor according to one embodiment of the present invention includes a pixel unit 10 and an output unit 20.

[0025]

The pixel unit 10 includes N line sensors 12_1 to 12_N each having M charge-coupled devices (CCDs) 14 arranged in a line, wherein the N pieces of line sensors 12_1 to 12_N are horizontally arranged in a scan direction, horizontally move charges accumulated in respective columns of line sensors 12_1 to 12_N using a TDI method, and accumulate the charges.

[0026]

That is, as illustrated in FIG. 3, each of the charges accumulated in the CCDs 14 is moved to an adjacent CCD 14 by sequentially controlling voltages V1, V2, and V3 of each of the CCDs 14, overlaps a charge storage node FD, and is output.

[0027]

Since a configuration of the pixel unit 10 corresponds to a general configuration of a pixel unit of a TDI line image sensor, a detailed description of the configuration will be omitted in the present embodiment.

[0028]

The output unit 20 includes amplifiers 22, analog-to-digital (AD) converters 24, and a memory buffer 26 so as to receive charges accumulated in the pixel unit 10 from the respective columns in parallel as inputs, perform AD conversion on the charges to output a digital signal, store the digital signal, and then sequentially output the digital signal.

[0029]

In order to amplify each of the charges accumulated in the pixel unit 10 by receiving the charges from the respective columns in parallel to charge storage nodes FD as inputs, the amplifiers 22 include M amplifiers so as to correspond to the number of the CCDs 14 arranged in a single line sensor 12_1 to 12_N.

[0030]

In this case, the amplifiers 22 may be configured as source follower amplifiers in which charges are moved from a last line sensor 12_N of the pixel unit 10, the charges are turned on according to accumulated electric potentials of the charge storage nodes FD, and voltage values thereof are output.

[0031]

The AD converters 24 respectively perform AD conversion on signals output from the M amplifiers 22.

[0032]

The memory buffer 26 stores image signals converted into digital signals in the M AD converters 24, then sequentially outputs the image signals and allows a signal processing unit (not illustrated) to process the image signals for each line.

[0033]

When the TDI line image sensor configured in this way performs scanning and imaging, the charges accumulated in the CCDs 14 of each of the line sensors 12_1 to 12_N of the pixel unit 10 using a TDI method are synchronized with the scanning, are moved to an adjacent line sensor 12_1 to 12_N in respective columns thereof, and are output to the charge storage nodes FD of the output unit 20.

[0034]

After the charges accumulated in the charge storage nodes FD are amplified through the amplifiers 22, AD conversion is performed on the charges, and the charges are output as signals. Then, the charge storage nodes FD may be reset to have a voltage VDD connected to a reset drain RD through a reset gate RG, and may receive charges of a next line sensor 12_1 to 12_N as inputs.

[0035]

In this way, since the pixel unit 10 is configured in a TDI method through the CCDs, a high-resolution image having a sufficiently satisfactory amount of light may be obtained.

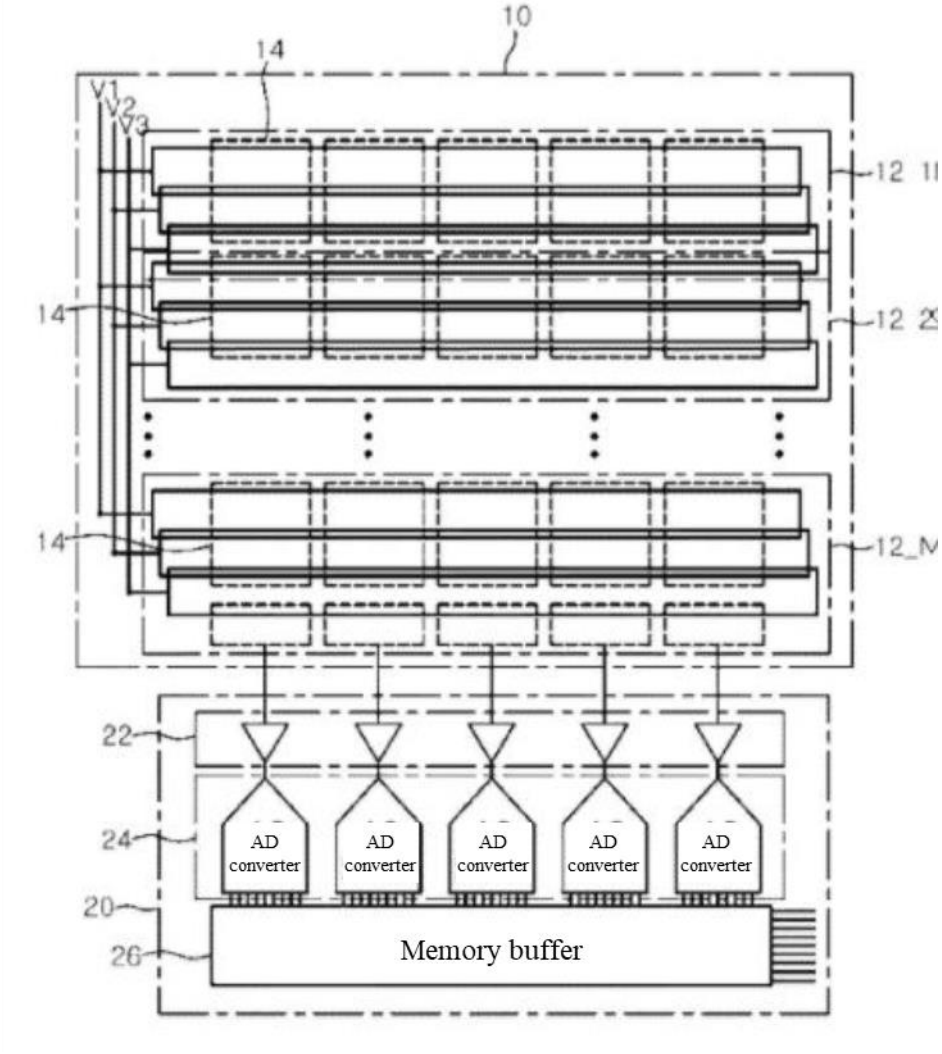
[0036]

Further, since the charges stored in the charge storage nodes FD of the output unit 20 are amplified through the amplifiers 22, are converted into digital signals in the AD converters 24, are stored in the memory buffer 26, and are then output without being moved through the CCDs, a degree of integration may be improved and a transmission rate may be improved even with less power consumption due to a complementary metal-oxide-semiconductor (CMOS) device.

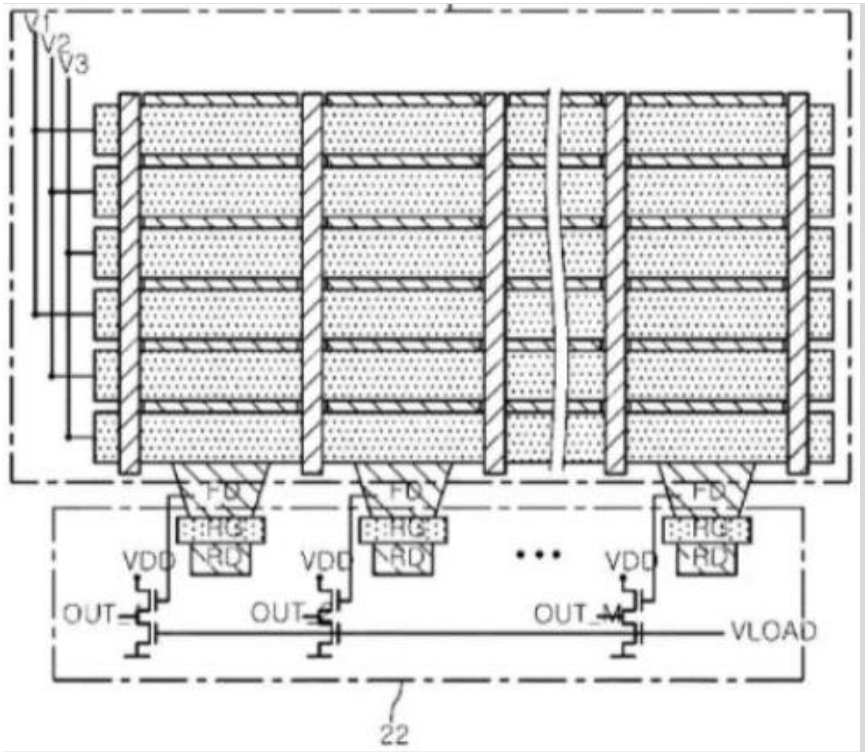
[0037]

As described above, in the TDI line image sensor according to the embodiment of the present invention, since the pixel unit is configured to accumulate charges through the CCDs in a TDI method and the output unit is configured to perform AD conversion on the charges accumulated in the CCDs in each column, store the charges in the memory buffer, and then sequentially output the charges, resolution and a transmission rate may be improved and power consumption and noise may be reduced due to characteristics of a CCD and a CMOS device.

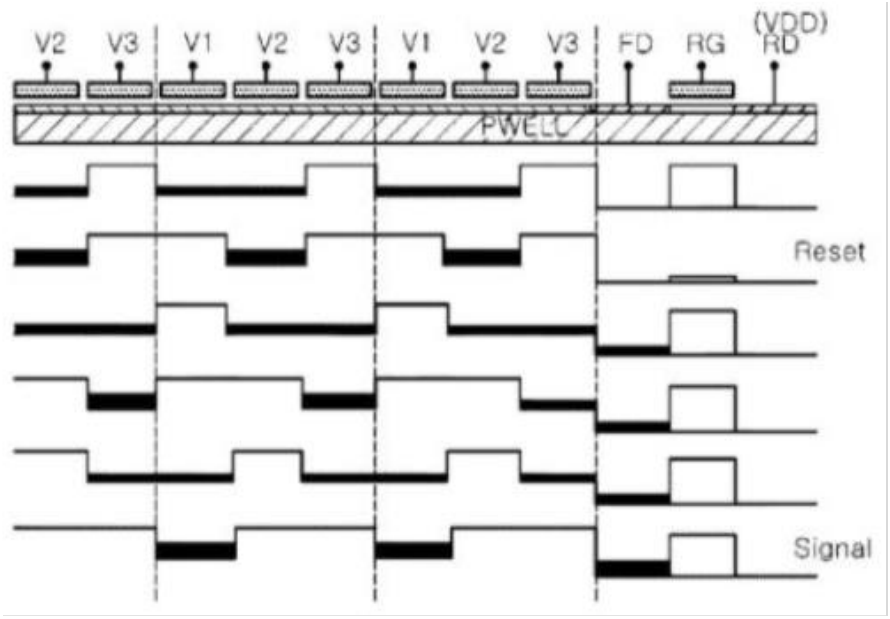
[FIG. 1]


10
14
V1
V2
V3
12 1
14
12 2
14
12_M
22
24
AD converter
AD converter
AD converter
AD converter
AD converter
20
26
Memory buffer

[FIG. 2]


V1
V2
V3
FD
RG
RD
VDD
OUT
VLOAD
22

[FIG. 3]


V2
V3
V1
V2
V3
V1
V2
V3
FD
RG
RD
(VDD)
PWELL
Reset
Signal

(Attachment 2)

(First column, line 19 through line 30)
BACKGROUND

Imaging devices are useful in a large number of applications. Particularly in the field of devices operating in remote locations and/or used in connection with the sending of image data in real time or near real time, focal plane arrays including photon detectors capable of producing an electrical signal in response to sensing photons have been developed. Of the various technologies produced for use with such focal plane arrays, charge coupled devices (CCDs) have proven to provide exceptional optical performance. Therefore, high performance photon detectors often feature a CCD sensor.

(First column, line 31 through line 35)

Additionally, in the field of aerospace sensors, Time Delayed Integration Charge Coupled Devices (TDI CCDs) are uniquely suited to on orbit observations due to their nearly noiseless charge transfer and summing capability combined with an orbital motion that scans the image across the sensor.

(First column, line 36 through line 47)

CCDs, however, are characterized by relatively high power consumption. For devices in which high power consumption is a concern, devices formed using other processes, such as Complimentary Metal Oxide Semiconductor ["Complimentary" contained in the original text is a clerical error for "Complementary"] (CMOS) devices, are preferable. In particular, the technology required to produce low power consumption, densely packaged processing circuitry using CMOS technology is well developed. However, CMOS photon sensors typically produce a noisier signal than do CCD devices, and generally have less desirable optical performance. In addition, it is more difficult to perform the function of Time Delayed Integration (TDI) in a purely CMOS photon sensor.

(First column, line 48 through line 60)

Accordingly, it would be desirable to create a photon sensor in which the exceptional optical performance of a CCD photon detector was combined with the low power consumption and dense circuitry packaging available using CMOS processes. Combining the CCD and CMOS processes on a single substrate, however, has proven difficult. Such difficulties arise from fundamental incompatibilities between the two

processes, including different processing temperatures and required oxide thicknesses. In addition, devices created on a single substrate using both CCD and CMOS technologies can suffer from poor image quality because of charge transfer inefficiency and high noise due to non-optimized processes.

(First column, line 61 through second column, line 2)

In order to avoid integrating incompatible fabrication process technologies, devices that utilize a structure formed on a first substrate using a first process (e.g. a CCD photon detector) interconnected to a second substrate using a second process (e.g. a CMOS readout) have been developed. Such systems have typically sensed or read an amount of charge from the detector (first) substrate, and have then amplified the charge on the readout and processing (second) substrate to obtain a signal that can be used to create an image.

(Second column, line 3 through line 7)

Additionally, it should be noted that charge detection generally can be performed only once with respect to a particular collection of charge. Also, providing an un-amplified or un-buffered signal from the CCD can in many cases result in a degraded signal.

(Second column, line 9 through line 12)

SUMMARY

The present invention is directed to solving these and other problems and disadvantages of the prior art.

(Second column, line 13 through line 28)

At least one embodiment of our invention is based in part on the fact that the power dissipation in a CCD can be dramatically reduced by extracting data from the CCD at or near the column (parallel) outputs thus removing the power intensive serial shift registers. Thus the combination of a CCD photon detector with column parallel voltage outputs driving a CMOS readout circuit including digitization and possibly data processing would provide significant advantages over the present state of the art. Our invention accordingly relates to combining separately fabricated CCD photon detectors incorporating voltage outputs with CMOS readout circuits into a single photodetection system. In many cases, this involves mechanically and electrically bonding the detector substrate to the readout circuit substrate using state of the art techniques. Note that in

some cases, others may refer to columns as rows and vice versa.

(Second column, line 29 through line 49)

In accordance with embodiments of the present invention, a photon sensor system is provided that includes a charge coupled device (CCD) photon detector on a first semiconductor substrate that is associated with a sense node. The sense node of the first semiconductor substrate is electrically interconnected to a readout circuit on a second semiconductor substrate. In particular, the charge coupled device sense node provides a voltage signal to the readout circuit across the electrical interconnection. The first semiconductor substrate may comprise structures formed in silicon or other semiconductor material, while the second semiconductor substrate may comprise semiconductor structures that are different than the structures of the first semiconductor substrate. In accordance with embodiments of the present invention, the electrical connections may form signal lines and may comprise bump bonds, wires, vias, or traces that may in certain embodiments be formed on a third substrate. In accordance with still further embodiments of the present invention, the first and second semiconductor substrates are mechanically interconnected to one another, either directly or through a third substrate.

(Second column, line 50 through line 59)

The sense node, also known as an output node, on the first semiconductor substrate may be buffered by one or more transistors on the first or photon detector substrate, before a signal is transmitted to the readout circuit on a second semiconductor substrate. As an example, the transistor or transistors may comprise or be part of an amplifier comprising a source follower formed on the CCD (first semiconductor substrate). As a further example, the transistor or transistors may comprise or be part of a voltage mode amplifier formed on the CCD.

(Second column, line 60 through third column, line 3)

In accordance with still other embodiments, a charge to voltage amplifier may be provided on the CCD. In accordance with other embodiments of the present invention, a voltage signal from the sense node is passed to the readout circuit on the second semiconductor substrate, without amplification on the first semiconductor substrate. The readout circuit on the second semiconductor substrate that receives the voltage signal may comprise a voltage amplifier, a voltage comparator, a buffer or an analog to digital converter. Moreover, the voltage of the sense node may be read using various

techniques, including the use of correlated double sampling.

(Third column, line 4 through line 24)

In accordance with embodiments of the present invention, methods for sensing light may include creating an electrical charge in response to detecting photons using a CCD fabricated on or comprising a first semiconductor substrate. Moreover, the first semiconductor substrate may comprise a silicon semiconductor. A first collection also known as a first packet of charges including all or some proportion of the electrical charge created in response to detecting photons is collected in a first potential well. A voltage signal is subsequently generated by reading a first voltage associated with the first packet (collection) of charges deposited in the first potential well. The first voltage signal is provided to a first circuit component formed on a second semiconductor substrate, and the first voltage signal is processed using circuitry including the first circuit component on the second semiconductor substrate. In accordance with still other embodiments of the present invention, a second voltage signal is created by reading a second voltage associated with the first packet of charges deposited in the first potential well. That is, a voltage associated with a first packet of charge deposited in a potential well on the first semiconductor substrate can be read multiple times.

(Sixth column, line 50 through seventh column, line 43)

FIG. 6 is a cross-section showing some features of a first semiconductor substrate 126 comprising an imaging sensor array 124 in accordance with the embodiments of the present invention. As shown, the imaging sensor array 124 includes a plurality of pixels or means for detecting light 604 formed in the semiconductor substrate 126. In addition, the imaging sensor array 124 includes a readout or summing well 608 for improved noise performance and a sense node (output node) 804, from which a voltage signal may be provided to readout circuitry 128 (not shown in FIG. 6) formed on a second semiconductor substrate 130. Moreover, the sense node 804 typically comprises a contact to the floating diffusion. Other embodiments may not employ a summing well 608. In general, and as can be appreciated by one of skill in the art, each pixel 604 comprises a photo sensitive area. More particularly, in response to photons incident on a pixel 604, a charge is accumulated. Moreover, within the effective sensitivity range of a pixel 604, the amount of accumulated charge depends on the number of photons received at the pixel 604 during an integration period. As can also be appreciated by one of skill in the art, the pixels 604 illustrated in FIG. 6 may comprise a linear array or one column (or row) within an area array or sub-array included in an imaging sensor

array 124 in accordance with embodiments of the present invention. Accordingly, after an integration period, collected charge may be transferred from one pixel 604 to the next in series and finally, for embodiments in which a summing well is not employed to the last well 614. In other embodiments, charge may be accumulated in successive pixels 604 during successive integration periods. Substantially all of this accumulated charge is then transferred into the last well 614. This process is also known to those skilled in the art as Time Delayed Integration (TDI). Again, a summing well 608 may be used just before the sense node 804 for improved noise performance. Although FIG. 6 shows 3-phase clocking, other embodiments may utilize 4-phase or another number of phase clocking. More particularly, once each collection of charge is deposited in the last well 614, the charge is moved from the last well 614 to the sense node 804 to read out a voltage signal 612 which is transmitted to readout circuitry 128 (not shown in FIG. 6). Alternatively, in embodiments in which an amplifier (e.g. a buffer or a CTIA (Capacitance Transimpedance Amplifier)) is provided on the first semiconductor substrate 126, either a voltage or a charge signal may be read from the sense node 804, and a voltage signal 612 may then be provided by the output of the amplifier. In general, movement of charge between pixels is accomplished using transfer gates 620. The last gate (output gate) 622 functions to isolate the sense node from the last well or in cases in which it exists, the last gate 622 functions to isolate the sense node from the summing well. Although the sense node 804 is depicted adjacent to the voltage signal 612, it can be appreciated that intermediate circuitry may be provided in accordance with embodiments of the present invention. As can be appreciated by one of skill in the art, intermediate circuitry may be interposed between the sense node 804 and the output voltage signal 612, forming a part of the output. In addition, multiple sense nodes 804 may be associated with a column (row) of pixels 604. In one embodiment, sense nodes 804 may be present at both ends of a column (row) of CCDs and used for forward or reverse operation of the CCD.

(Seventh column, line 44 through eighth column, line 13)

FIG. 7 is a schematic depiction of components of a hybrid imager 120 in accordance with embodiments of the present invention. Two columns (rows) 702a-b of pixels 604 comprising the photo-sensitive area of the imaging sensor array 124 are depicted, with each column (row) 702 interconnected to a sense node 804. First and second interconnections 404a-b provide voltage signals from the first and second sense nodes 804 to the inputs of pre-amplifiers 708 formed on the second semiconductor substrate 130, and comprising part of the readout circuitry 128. As illustrated, each sense node

804 may be associated with a single pre-amplifier 708, although other arrangements are possible. Moreover, because the pre-amplifiers 708 comprise voltage mode amplifiers and are provided with a voltage signal from the sense nodes 804 by the interconnections 404a-b, the voltage of the sense nodes 804 can be read multiple times to provide multiple measurements of a single collection of charge. Accordingly, multiple samples (measurements) can be taken of the charge in or associated with a sense node 804 in order to improve the signal to noise ratio. One or more additional amplifiers 712 may also be provided as part of the readout circuitry 128. As illustrated in FIG. 7, the input to such additional amplifiers 712 may comprise the output from one or more of the pre-amplifiers 708. A switch 716 may be provided so that amplifier 712 may selectively receive its input from either of the amplifiers 708. Because this additional amplifier 712 receives input from at least one other amplifier 708 included in the readout circuitry 128, the additional amplifier 712 may not necessarily be a voltage mode amplifier. The output from the additional amplifier 712 may then be provided to additional circuitry associated with another substrate or device for processing (including for example correlated double sampling (CDS) and analog to digital conversion), display or storage. Alternatively, such additional circuitry may be provided as part of the readout circuitry 128. For example, memory may be provided for temporary or long-term storage of image data collected by pixels 604 on the imaging sensor array 124.

(Eighth column, line 14 through line 35)

FIG. 8 is a schematic depiction of portions of a hybrid imager 124 including a sense node 804 that provides a voltage signal in accordance with the embodiments of the present invention. In particular, in the illustrated embodiment, the sense node 804 comprises a floating gate 806 overlaying a potential well 818. The transfer of charge to the potential well 818 from an adjacent potential well 812 may be controlled using control gates 816 sometimes also known as transfer or CCD gates. In particular, the potential well 818 can be set into depletion using bias gate 822. As charge associated with an image signal from one of the pixels 604 is transferred into the potential well 818, voltage changes on the gate 806 are introduced that can be sensed. For example, a voltage signal from the floating gate 806 may be provided to an amplifier or pre-amplifier 820 formed on the first semiconductor substrate 126 or on the second semiconductor substrate 130. After being sensed, the signal charge packets can be transferred out of the potential well 818 and removed through a diode 830 and a diode drain 832 or they can remain beneath the floating gate 806 to allow multiple samples for noise reduction. After the desired number of samples is obtained, the charge can

then be removed through the diode drain 832.

(Eighth column, line 46 through line 60)

Portions of a hybrid imager 124 in accordance with other embodiments of the present invention are illustrated in FIG. 9. In particular, FIG. 9 differs from the hybrid imager 124 depicted in FIG. 8 in that the voltage signal from the sense node 804 is provided using an electrode 904 that also functions as a floating gate. The voltage on electrode (gate) 904 is determined by the reset transistor 908. In addition, the signal line 906 for carrying the voltage signal from the sense node 804 to the voltage mode amplifier 820 is associated with a reset switch or transistor 908. The reset switch 908 and/or the voltage mode amplifier 820 may be formed on either the first semiconductor substrate 126 or the second semiconductor substrate 130. After being sensed (possibly multiple times), the signal charge packets can be removed through a diode drain (not shown in FIG. 9).

(Ninth column, line 22 through line 51)

FIG. 12 is a schematic depiction of portions of a hybrid imager 120 in accordance with embodiments of the present invention. The CCD imaging sensor array 124 includes a plurality of pixels 604 grouped in a plurality of sub-arrays 1204. Each column (row) of pixels 604 may be associated with a sense node 804a. In addition, a second sense node 804b at an end of each column (row) of pixels 604 opposite the end at which the first sense node 804a is located may be provided to support bi-directional output from the sub-arrays 1204. As illustrated, an amplifier 1208, formed on the first semiconductor substrate 126, may be associated with each sense node 804. For purposes of clarity of illustration, not every column (row) of pixels is shown with associated sense node 804 or amplifiers 1208, or other components subsequently described in connection with the figure. As can be appreciated by one of skill in the art, the amplifier 1208 need not provide an output voltage that is different than or amplified as compared to the voltage sensed from the sense node 804. Accordingly, the amplifier 1208 may comprise a source follower or other buffer to provide a voltage buffered output. In accordance with other embodiments of the present invention, the amplifier 1208 may read a charge signal from the associated sense node 804, and provide a voltage signal at the output of the amplifier. Accordingly, a charge to voltage conversion may be performed on the first semiconductor substrate 126 comprising the CCD imaging sensor array 124. Alternatively, the amplifier 1208 on the first semiconductor substrate 126 comprising the CCD imaging sensor may be omitted, in which case the voltage signal

is read from each sense node 804 directly.

(Ninth column, line 52 through tenth column, line 12)

The voltage signal from the sense node 804, whether it is read from the un-amplified collection of charge in the sense node 804 or is read from the output of an amplifier 1208 on the first semiconductor substrate 126, is provided to readout circuitry 128 formed on the second semiconductor substrate 130 by an interconnection 404. For example, the voltage signal from a pixel 604 of the CCD imaging sensor array 124 on the first semiconductor substrate 126 is communicated to the input of a voltage-mode amplifier or pre-amplifier 708 comprising at least a portion of the readout circuitry 128 formed on the second semiconductor substrate 130. The amplifiers 708 are shown in FIG. 12 using dotted lines because in the illustrated example they are located on a portion of the second semiconductor substrate 130 that underlies the first semiconductor substrate 126 in that figure. As can be appreciated by one of skill in the art, a voltage-mode amplifier is characterized by a high or an essentially infinite input impedance. As a result, the voltage of the sense node 804, as communicated to the input of the amplifier 708 by the interconnection 404, can be sampled or read multiple times. This is in contrast to a charge mode amplifier, which if connected to a sense node 804 directly would deplete the charge collected in the sense node 804, and therefore could be read from the sense node 804 only once. As can also be appreciated by one of skill in the art, the amplifier 708 need not provide an output voltage that is different than or amplified as compared to the input voltage. For example, the amplifier 708 may comprise a source follower or other buffer.

(Tenth column, line 13 through line 20)

As illustrated in FIG. 12, the first semiconductor substrate 126 may include a number of means for forming potential barriers, or control gates 816. As can be appreciated by one of skill in the art, control gates 816 may be provided for moving collected charge from a pixel 604 or sequentially from a column (row) of pixels 604 to a sense node 804. Also, reset switches 908 can be formed on the first semiconductor substrate 126 for resetting associated sense nodes 804.

(Tenth column, line 21 through line 57)

The readout circuitry 128 formed on the second semiconductor substrate 130, as previously noted, may include an amplifier or preamplifier 708. Alternatively or in addition, the readout circuitry 128 may include a CDS circuit 1000 to reduce low

frequency noise components, including 1/f noise. If bi-directional output is provided, the sense node 804 from which a voltage signal for a pixel 604 or pixels 604 included in a column (row) of pixels is obtained may be selected using a switch 1212 formed on the second semiconductor substrate 130. Additional amplification may be provided by column (row) amplifiers 1216. These amplifiers 1216 may comprise differential or single-ended amplifiers. In accordance with embodiments of the present invention, the signal from a pixel or the integrated signal from many pixels in a TDI arrangement is then processed by an analog to digital converter (ADC) 1220. As examples, an ADC may comprise a ramp ADC or a pipeline ADC. After data is digitized by an ADC, it can be digitally processed by a serializer 1224, also formed on the second semiconductor substrate 130. The output from the serializer can then be passed from the second semiconductor substrate 130 to other circuitry, for example for storage or display. Transfer of the digital data may be by a digital data link 1228. For example, the digital data link 1228 may comprise a low voltage differential signaling (LVDS) link. Clock generation may be provided by clock generation circuitry 1232 provided as part of the readout circuitry 128 on the second semiconductor substrate 130. In accordance with embodiments of the present invention, external circuitry 1236, or circuitry not formed on either the first 126 or second 130 semiconductor substrates, may be used to couple the clocking signals into the CCD sensing array 124 at the correct voltages. In other embodiments, the external circuitry 1236 may also be formed on the second semiconductor substrate 130. Although a number of circuits have been described as being formed on or as part of the second semiconductor substrate 130, some or all of these circuits may be omitted or formed on other substrates.

FIG. 8

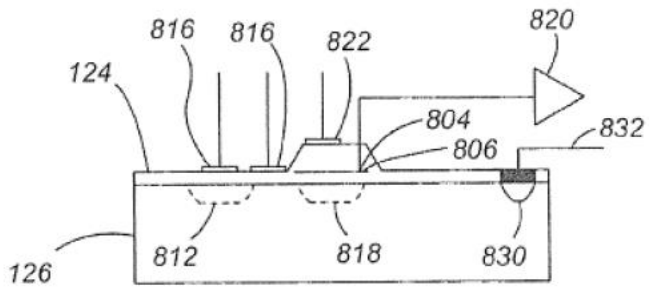
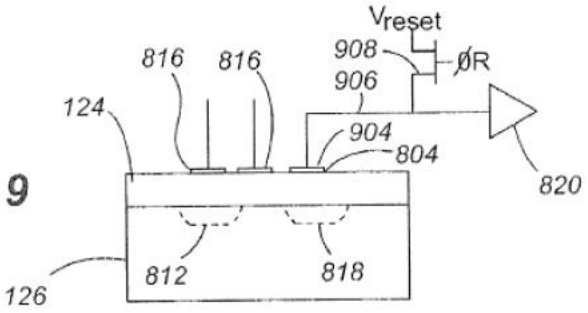


FIG. 9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Vreset
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ØR
906
816
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812
818
126

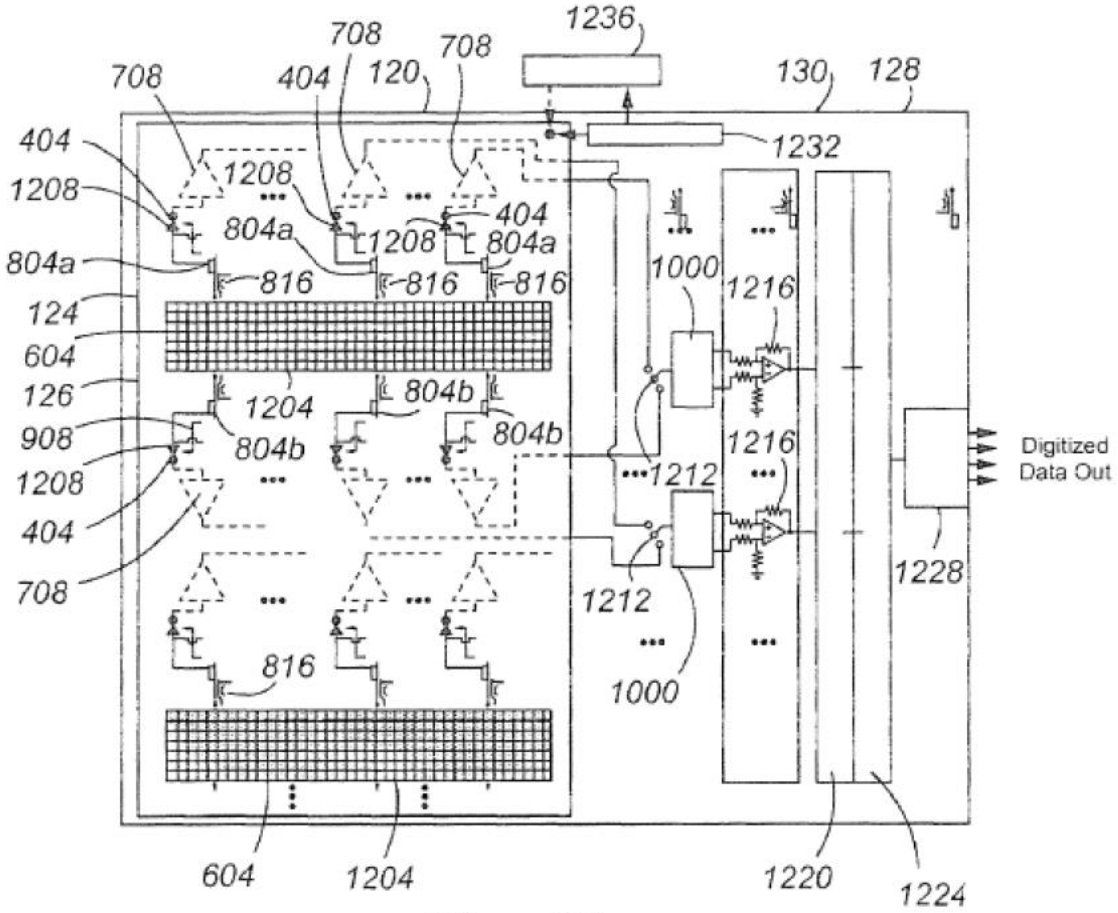

1236
708
708
708
404
120
130
128
1232
404
1208
1208
804a
804a
816
816
816
124
604
126
1204
804b
804b
908
804b
1208
404
708
1000
1216
1216
1212
1212
1000
816
1228
Digitized
Data Out
604
1204
1220
1224

Fig. 12

(Attachment 3)

1. Unexamined Patent Application Publication No. 1990-159737 (Exhibit Otsu 5)

(1) "[Prior art]

A CCD delay line comprising a charge transfer device is used for forming various color signals, luminance signals and other signals from video signals detected by a solid-state imaging device and a buried channel CCD is used in terms of transfer efficiency of signal charges and other reasons." (page 1, lower right column, line 3 through line 8)

(2) "Next, the third conventional example shown in FIG. 10 is called a floating gate type amplifier, and it is disclosed in Unexamined Patent Application Publication No. 1988-88864 and in other materials. Describing the principle schematically, in FIG. 10, a gate electrode 4, to which pre-determined DC voltage OG is applied at the end of BCCD1, a floating gate 5, gate electrodes 6 and 7 for resetting, and a drain D are formed sequentially. Constant voltage V_{DD} of a booster circuit 3 is applied to a drain terminal. The gate electrodes 6 and 7 for resetting discharge signal charges under the floating gate 5 to the drain D when they are synchronized with a reset signal φ_R at the pre-determined timing and turn on. Q_1 is a transistor for resetting that is associated between a power supply voltage Vcc and the floating gate 5. It resets the floating gate 5 to the potential equivalent to the power voltage Vcc when it is synchronized with a reset signal RST at the predetermined timing and turns on. (page 2, lower right column, line 4 through line 20)

(3) "[Example]

An embodiment example of the present invention is described below along with figures.

FIG. 1 is an embodiment configuration diagram showing the structure of the terminal part of the CCD delay line main body and the signal output means, and FIG. 2 and FIG. 3 show detailed circuit configurations of the signal output means.

In FIG. 1, an ion-implanted layer 11 of N^- type impurity is formed on the surface of a P-type semiconductor 10. A gate electrode for charge transfer is laminated through gate oxide film and thereby a buried channel CCD (BCCD) is formed in area A in the figure. The area A constitutes the main body of a delay element.

(omitted)

Next, to describe the configuration of the signal output means, reference numeral 20 denotes a potential detection circuit which detects voltage generated in the floating gate 17, and is formed of a voltage follower type circuit as shown in FIG. 2 or a circuit having a switched capacitor integrator as shown in FIG. 3.

In other words, the circuit shown in FIG. 2 has an MOS-type transistor Q_S wherein a gate contact is connected to the floating gate 17 and a source contact is connected to a power supply terminal V_{cc}; an MOS-type transistor Q_6 that is connected for opening and closing between the gate contact and power supply terminal V_{cc} by applying a reset signal RST to the gate contact; and the MOS-type transistor Q_6 wherein a source contact is connected to the drain contact of a transistor Q_5, the drain contact is connected to an earth terminal, and the pre-determined bias voltage V_{GS} is applied to the gate contact. In addition, the drain contact of the transistor Q_5 is connected to an analog switch SW1 through a buffer amplifier AMP1; and the output contact of the analog switch SW1 is connected to the earth terminal through a capacitance element C_1 and also connected to an output terminal OUT through a buffer amplifier AMP 2.

Here, the reset signal RST is to reset the floating gate 17 to the potential of the power supply terminal V_{CC} at the pre-determined timing. The analog switch SW1 opens and closes by synchronizing with a sample and hold signal SH and, thereby, has a capacitance element C_1 sample and hold the voltage of the floating gate 17, and, furthermore, generates voltage maintained in the capacitance element C_1 at the output terminal OUT through the buffer amplifier AMP 2, and thereby outputs changes in charges occurred at the floating gate 17 as changes in voltage." (page 4, upper left column, line 3 through lower left column, line 16)

(4) "The operation of an embodiment example related to the following composition is described based on the timing chart of FIG. 5 and the potential profile of FIG. 6. FIG. 6 corresponds to the explanatory diagram of composition of FIG. 1 and shows the potential profile of FIG. 5 at an appropriate time point.

First, the floating gate 17 is reset to a pre-determined potential at the beginning of each cycle in order to read each signal charge transferred at a pre-determined cycle in synchronization with the transfer clock signals φ_1 and φ_2. For example, the reset signal RST is temporarily set at "H" level at a time point t_1 in a cycle, and, thereby, the circuit in FIG. 2 is reset to the potential of power supply voltage V_{cc} (e.g., 5 volts) by electrically connecting the transistor Q_4 and the circuit in FIG. 3 is reset to the potential of bias voltage V_B (e.g., 3 volts) by electrically connecting the analog switch SW2. Further, a rectangular control signal φ_{RST} (e.g., 0 volts and 5 volts) which is inverted in the same phase as the reset signal RST lowers a potential barrier under a gate electrode 18 as shown in FIG. 6 (a) at time point t_1 and discards unnecessary charges under the floating gate 17 to an impurity layer 19. Then, when the reset signal RST and the control signal φ_{RST} reach "L" level again, the floating gate 17 is held at an initialization potential in a high impedance state, and the potential barrier under the gate electrode

18 becomes high.

At time point t_1 of the initialization, as shown in FIG. 6 (a), the signal charge q_1 located at the most output side is transferred to under gate electrodes 14 and 15, the next signal charge q_2 is transferred to under a gate electrode 30, and the next signal charge q_3 is transferred to under a gate electrode 26.

Next, at time point t_2, a clock signal φ_{1A} and a clock signal φ_{2B} reach "L" level and a clock signal φ_{2A} reaches negative "L" level, and thereby, as shown in FIG. 6 (b), potentials under gate electrodes 29, 30, 14, and 15 become shallow. Then, the signal charge q_1 exceeds a potential barrier under a gate electrode 16 and is transferred to under the floating gate 17 and the signal charge q_2 is transferred to under gate electrodes 31 and 13 and under an impurity layer 12. As a result, the potential of the floating gate 17 changes in proportion to the signal charge q_1. In the case of a circuit in FIG. 2, a voltage signal SC_1, which corresponds to the potential of the floating gate 17, is generated at the output contact of the buffer amplifier AMP1. In the case of a circuit in FIG. 3, a voltage corresponding to the potential of the floating gate 17 is held in the capacitance element C_3, and, at the same time, the voltage signal SC_1, which is equivalent to the voltage held, is generated at an output contact of a differential amplifier AMP3.

Next, at time point t_3, the clock signal φ_{1A} reaches "H" level, and the signal charge q_2 is transferred to under the gate electrode 14, and, in addition, at time point t_4, the clock signal φ_{2B} reaches "H" level and the signal charge q_2 is transferred to under a gate electrode 15 and, at the same time, transfers signal charge q_3 for the portion of the next one pixel, which is transferred from the BCCD by synchronizing with clock signals φ_1 and φ_2, to under gate electrodes 29 and 30.

In addition, when the sample and hold signal SH reaches "H" level between time points t_3 and t_4, in the circuit of FIG. 2, the output signal SC_1 is held in the capacitance element C_1, and in the circuit of FIG. 3, the output signal SC_1 is held in the capacitance element C_3, and the respective circuits generate a signal S_0 proportional to the voltage held to the output terminal OUT.

Thus, reading of the signal charge q_1, which has been transferred to under the gate electrodes 14 and 15, is completed by the processing at time points t_1 through t_4.

Next, at time point t_5, the reset signal RST is set to "H" level and the control signal φ_{RST} is set to "H" level. Then, as shown in FIG. 6 (d), the height of the potential barrier under the gate electrode 18 is lowered, and, at the same time, the potential under the floating gate 17 is set to the pre-determined initial level, the signal charge q_1 is discarded into the impurity layer 19, and the initialization is performed in the same way

as shown in FIG. 6 (a).

In addition, at time point t_5, a signal φ_{1A} is set to "L" level, and a signal charge q_2 is transferred only to under the gate electrode 15. In addition, at time point t_6, the signal φ_{2B} is set to "L" level and a signal charge q_2 is transferred to under the floating gate 17.

Then, at time point t_6, a signal charge q_2 that is transferred to the floating gate 17 is detected in the same way as the aforementioned signal charge q_1 and a voltage signal S_0, which is equivalent to the signal charge q_2, is output. In this way, the reading process of the signal charge q_2 is completed.

The signal charge q_3, which was under the gate electrode 26 at time point t_1, is transferred to under the gate electrode 30 during time points t_1 through t_6, and undergoes the same reading process as above.

These operations synchronize with cycles of clock signals φ_1 and φ_2 of the BCCD and are implemented repeatedly, and signals for every delayed stage can be output." (page 5, lower right column, line 5 through page 6, lower right column, line 18)"

(5) FIG.1

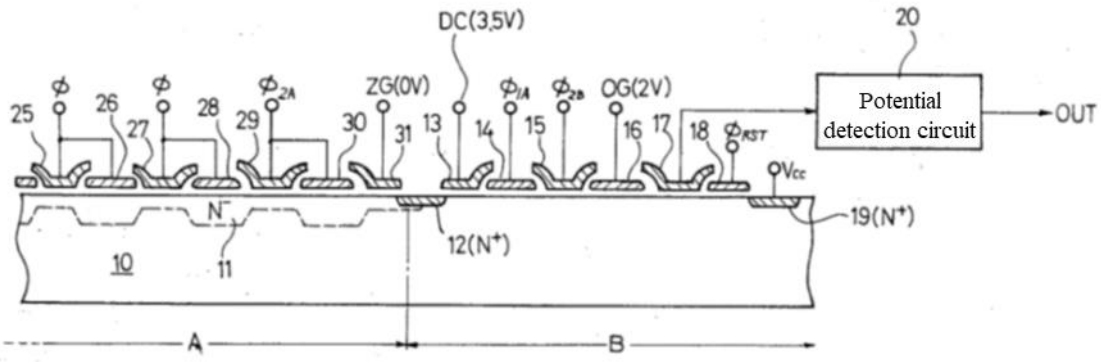


FIG. 2

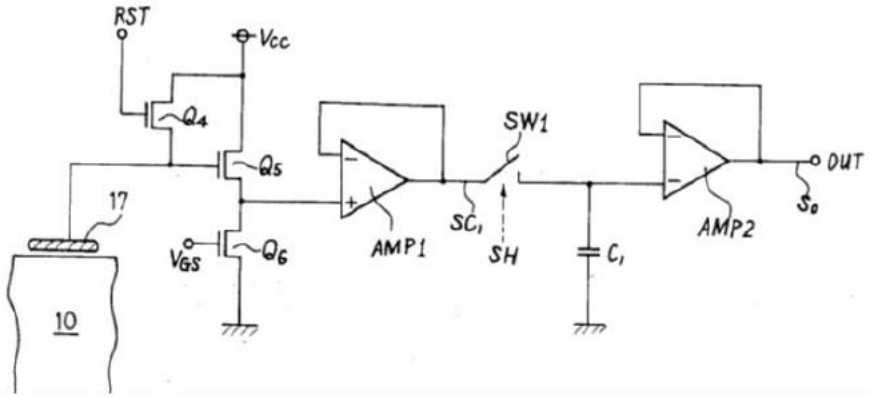
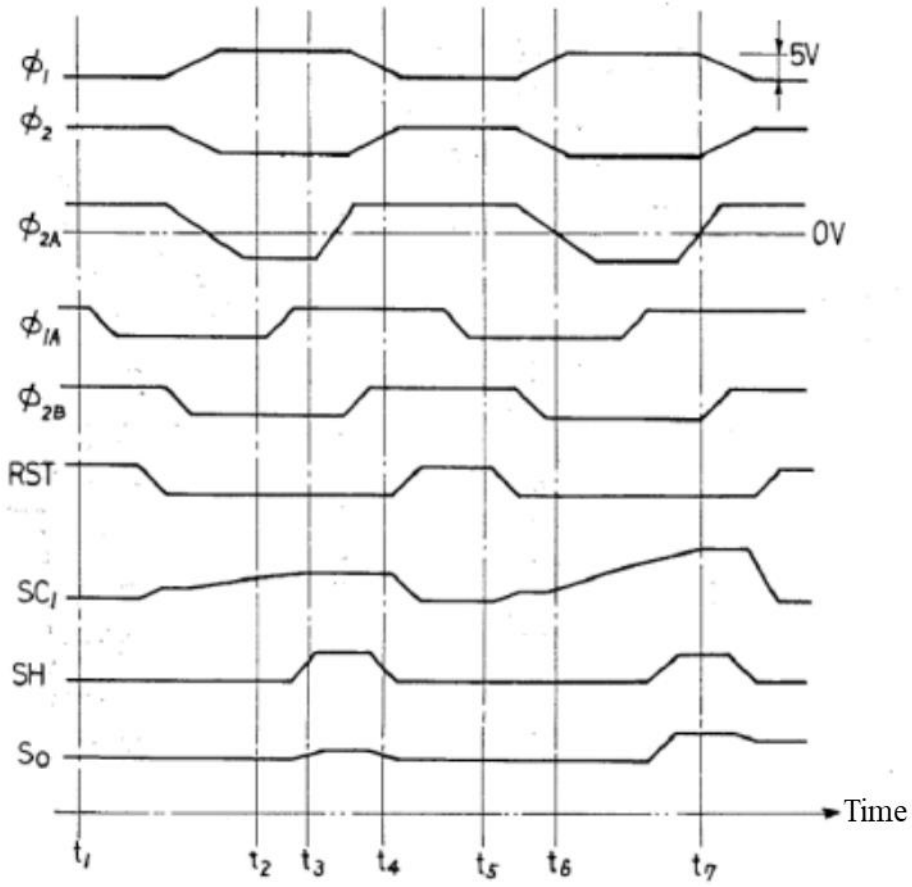


FIG. 5


ϕ_1
ϕ_2
ϕ_{2A}
ϕ_{1A}
ϕ_{2B}
RST
SC_1
SH
S_O
5V
0V
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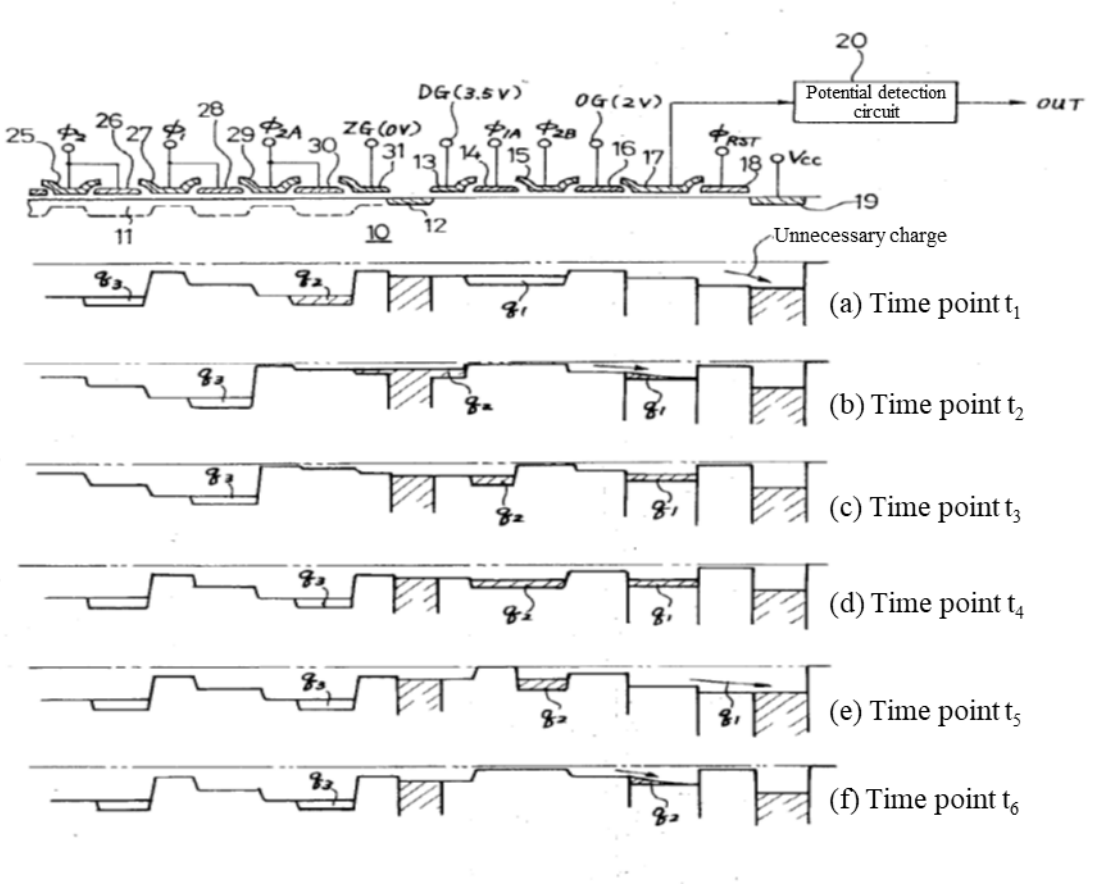
t_6
t_7

FIG. 6



2. Unexamined Patent Application Publication No. 1995-161969 (Exhibit Otsu 6)

[0002]

[Prior art] In CCD, it is necessary to detect low noise from a signal charge and to amplify the signal charge. Representative charge detection devices of CCDs are floating diffusion amplifiers (hereinafter referred to as "FDA") and floating gate amplifiers (hereinafter referred to as "FGA"). FDAs are the most disseminated and FIG. 9 shows the overall structure of an existing CCD that uses an FDA. Photons entering a photo diode (PD) 90 are converted into charges and accumulated in the PD 90. After a certain period of time, the signal charges are read out to a VCCD 91, are input into an FDA 93 through an HCCD 92, and are detected as a voltage. In this FDA, there is a problem that reset noise occurs. On the other hand, FGAs have a feature that an amplifier without a reset noise can be realized in a non-destructive manner.

[0004] FIG. 10 is a diagram indicating the parasitic capacitance of a conventional FGA and shows a cross section of a case where a signal charge Q is input under a floating gate (FG) 95. A FG 95 is formed with polysilicon on an Si substrate with a gate oxide

film 96 interposed therebetween. After an insulating film is formed using SiO_2, a bias gate 94 is formed with aluminum or tungsten. At this time, C1 is the capacity between the signal charge Q and the FG95; C2 is the capacity between the FG95 and a BG94; C3 is the depletion layer capacity between the signal charge Q and a P-type substrate; C4 is a capacity between the FG95 and a P+ region (functions as a channel stopper); and C5 is the input capacity of a MOS transistor (hereinafter referred to as "Tr"). The MOSTr constitutes a source follower (not shown in the figure) and converts the signal voltage into a low output impedance and outputs it. In other words, the FG 95 serves both as the gate for charge detection and as the gate of the first stage Tr. When the signal charge Q is input under the FG 95 in the presence of such parasitic capacitance, a voltage change of ΔV appears in the FG 95 according to equation (1).

[0007] FIG. 11 is a plan view and a cross sectional view of the periphery of a conventional FGA. Signal charges are transferred by applying φ H1 and φ H2 to gates formed on an HCCD 92. Signal charges are transferred to under the FG95 over an output gate (OG) 97, and a charge voltage conversion is performed. The signal charge Q, which is detected at the FG 95, is discharged to a reset drain (RD) 99 in the same way as FDAs by a reset gate (RG) 98. As is apparent from FIG. 11, the FG 95, OG 97, and RG 98 overlap. This is because the FG95 is arranged in the same way as the gate to which φ H1 and φ H2 are applied. A capacity of C6 is newly added between the FG95 and the OG97, and a capacity of C7 is newly added between the FG95 and the RG98. Thus, conventionally, the sensitivity of FGAs is lower by 40 to 50 % than that of FDAs.

[0032] Next, the fifth embodiment example of the present invention will be described with reference to the figures. FIG. 5 is a cross sectional view, a potential diagram, and a timing chart of the periphery of an FGA in the fifth embodiment example of the present invention. A feature of the fifth embodiment example is that it does not form a reset gate and performs reset operation by applying the same phase of pulse as φ H1 to a reset drain. FIG. 5 (a) is a cross-sectional view and has a composition in which the reset gate is removed. There is a clearance between an FG30 and an RD99, and a BG94 does not completely cover the clearance. FIG. 5 (b) shows a potential diagram in this condition. If a low-level driving signal (not zero) is applied to the RD99, there is a potential gap between the FG30 and the RD99.

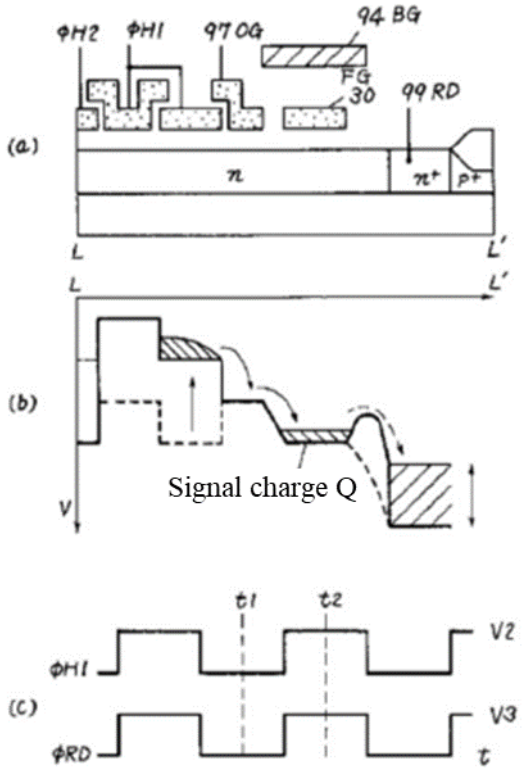
[0033] FIG. 5 (c) is a timing chart showing a relationship between φ H1 and φ RD (signals applied to a reset drain). FIG. 5 (b) shows a state at t1 in a solid line and a state at t2 in a broken line. Since the high-level signal (V3) is applied at t2, the potential gap disappears and the signal charge Q that has already been transferred to under (t1) FG30 is absorbed (reset) by the RD99. At this time, φH1 and φRD are in the same phase, but

the high levels (V2, V3) of the driving signal are different. The conventional reset pulse width has to be set to approximately half of the high period of φH1; however, in the fifth embodiment example, since it may be equivalent to φH1, the driving circuit becomes simple. In addition, since there are no reset gates, extra parasitic capacitance can be reduced, and charge detection sensitivity is improved. Needless to say, if the fifth embodiment example is applied to an FDA, the same effects can be obtained.

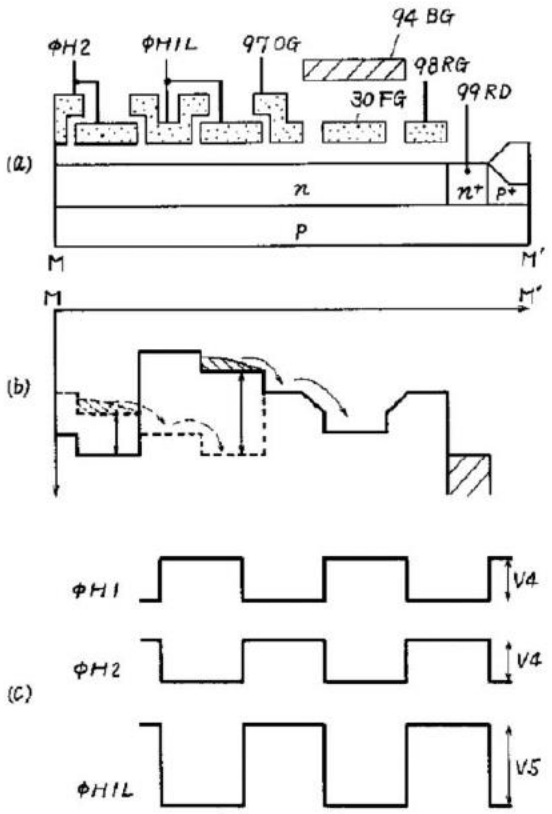
[0034] Next, the sixth embodiment example of the present invention will be described with reference to the figures. FIG. 6 is a cross sectional view, a potential diagram, and a timing chart of the periphery of an FGA in the sixth embodiment example of the present invention. A feature of the sixth embodiment example is to make the signal amplitude that is applied to φH1L (the last gate of the HCCD) adjacent to the OG97, bigger than the signal amplitude that applies to another φH1.

[0035] FIG. 6 (a) is a cross sectional view but differs from the conventional one in that a different signal is applied only to the final stage of φH1. FIG. 6 (c) is a timing chart and is a signal to be supplied to a charge detection device having the composition shown in FIG. 6 (a). FIG. 6 (b) is a potential diagram at this time. A pulse, wherein the signal amplitude is V4, is applied to φH1 and φH2, and a pulse, wherein the signal amplitude is V5, is applied to φH1L (V4<V5). Since the signal amplitude of φH1L is big, even if the OG97 potential is set lower than before, a CCD can be operated. Consequently, even if the potentials of the BG94 and the FG30 are lowered, a CCD can be operated. Therefore, the occurrence of leakage current is greatly suppressed and the FG potential is hardly changed. Needless to say, even if the sixth embodiment example is applied to an FDA, the CCD can be operated.

[FIG. 5]


φH2
φH1
97 OG
94 BG
FG
30
99 RD
(a)
n
n+
p+
L
L'
L
L'
(b)
V
Signal charge Q
t1
t2
V2
φH1
(c)
V3
φRD
t

[FIG. 6]



3. Unexamined Patent Application Publication No. 2008-60097 (Exhibit Otsu 7)

[0003]

As a main charge detection method other than the FD, there is a floating gate (hereinafter referred to as "FG,"; FG is an abbreviation for Floating Gate) method. The FG method is mainly used as a charge detection unit of a CCD element. The FG method has a composition, for example, wherein, at the end of a vertical CCD of a CCD imaging sensor, when a signal charge is transferred to a CCD channel under a floating gate for charge detection, which is reset to a certain potential, an FG potential changes based on signal charge amount, and the FG is connected to a gate of output MOSFET (FET: Field Effect Transistor). It is based on a principle where output MOSFET channel current is modulated based on the signal amount. According to this method, based on the fact that a transistor for resetting the FG unit is connected and the relationship with the area of the FG unit, charge detection capacity becomes greater more easily than the FD method and it is hard to obtain a charge detection unit with high conversion efficiency. However, since it is easy to set the output unit operation voltage in the second sentence at low level and it is read out in a non-destructive manner, there are advantages, such as where

a means for improving SN of the detection circuit by arranging a plurality of FGs can be taken.

[0013]

First, an outline of a solid-state imaging device will be described as an example of a CCD solid-state imaging device. As shown in FIG. 3, a solid-state imaging device (CCD solid-state imaging device) 1 includes an image unit 13 having a photoelectric conversion unit 11 for photoelectrically converting incident light and a vertical transfer unit 12 for vertically transferring a charge obtained by photoelectric conversion in the photoelectric conversion unit 11, a horizontal transfer unit 14 for horizontally transferring a vertically transferred signal charge to the output side, and an output unit 15 for converting the signal charge output from a horizontal transfer unit 24 into a voltage and amplifying the signal charge.

[0014]

Details of the output unit 15 above are as shown in FIG. 1 and FIG. 2 and a horizontal transfer unit (e.g., a horizontal transfer CCD) 14 is formed on a semiconductor substrate 10. The horizontal transfer unit 14 has a composition, wherein transfer gates 23 are arranged on a channel region 21 formed on a semiconductor substrate 10 through an insulating film 22, and each transfer gate 23 is connected to each vertical transfer unit, which are not shown in the figures. An output gate (horizontal output gate) 24, signal charge detection unit 25, and reset gate 26 are sequentially formed on the semiconductor substrate 10 on the output side of the horizontal transfer unit through the insulating film 22. The signal charge detection unit 25 consists of, for example, a driving transistor 31.

[0017]

In addition, the reset gate 26 is arranged at an interval in the traveling direction of the signal charge of the control gate 35. A reset drain 27 is formed on the semiconductor substrate 10 on the opposite side to the driving transistor 31 of the reset gate 26.

[0018]

In the solid-state imaging device 1, when the signal charges, which were transferred through the horizontal transfer unit 14, are transferred to a channel region 21 under a control gate 35 through the channel region 21 under the horizontal output gate 24, a potential change based on signal charge amount occurs in the channel region 21. The potential change that occurred in the channel region 21 modulates the potential of the channel 32 of the driving transistor 31 by capacitive coupling. The current-voltage (I-V) characteristics of the driving transistor 31 show the same trend as the current-voltage (I-V) characteristics of the MOSFET. Therefore, the channel region 21 functions as a

gate electrode unit of the driving transistor 31. Consequently, the current flowing through the driving transistor 31 is modulated and converted into a signal voltage, and is output to the outside as a signal output through a source follower.

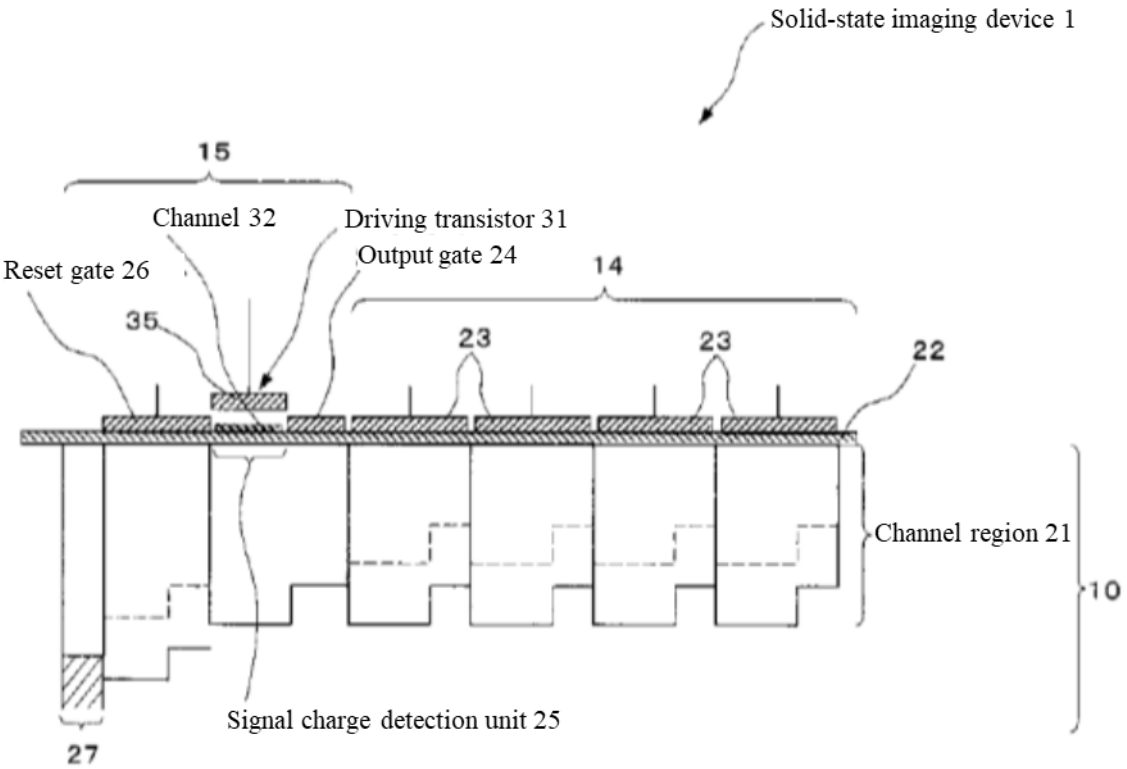
[0019]

In this embodiment example, after the signal charge is read out, the reset gate 26 is set to High, and charges are discharged from the channel region 21 to a reset drain 27. The reset operation can be changed to an operation to promote the complete transfer from the channel region 21 to the reset gate 26 by providing a potential to the Low side to the control gate 35 and by shallowing a potential of the channel region 21.

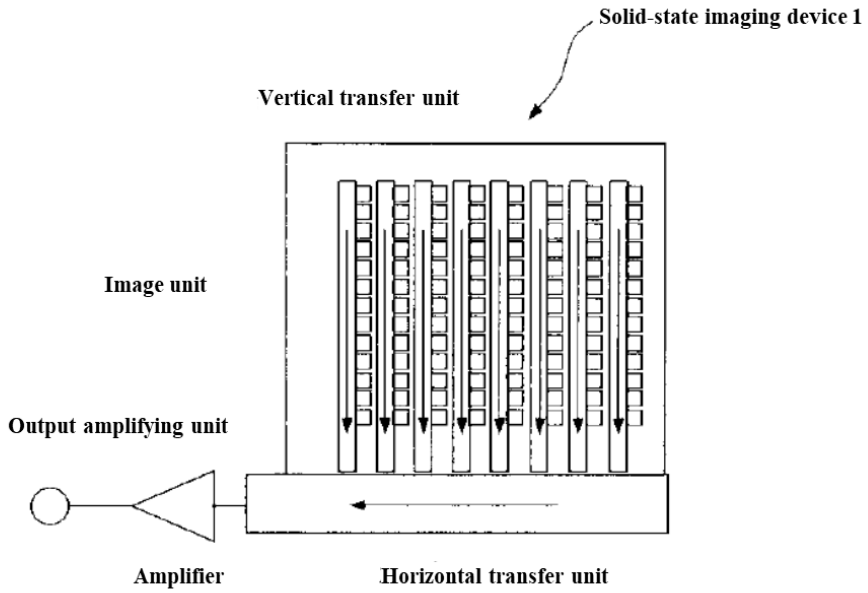
[0020]

In the solid-state imaging device 1, the signal charge detection unit 25 is continuously formed through the horizontal transfer unit 14 and horizontal output gate 24, and charge transfer from the signal charge detection unit 25 to the reset gate 26 is performed by a CCD transfer (complete transfer). For this reason, it has no KTC noise or charge sharing noise, and, therefore, high sensitivity can be achieved. In addition, although the solid-state imaging device 1 is basically a type of a solid-state imaging device using an FG method, it is possible to obtain a higher conversion gain than the FG method.

[FIG. 1]


Solid-state imaging device 1
15
Channel 32
Driving transistor 31
Output gate 24
Reset gate 26
14
35
23
23
22
Channel region 21
10
Signal charge detection unit 25
27

[FIG. 3]


Solid-state imaging device 1
Vertical transfer unit
Image unit
Output amplifying unit
Amplifier
Horizontal transfer unit